daPIPE Data Plane Incremental Programming Environment

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To set the context

Let's look into deployment options for programmable switches



Turn-key Deployment

- · Deployment as usual
 - · Familiar features and interfaces
- Resource optimization
- Future proof
- Feature agility
- Streaming telemetry

Platform vendor (Cisco)
 Chip vendor (Barefoot)
 Customer/open source

- No flexibility
- No custom feature and protocol support



Programmable chip

Hybrid Deployment

Best of breed



- Deployment as usual
 - Familiar features and interfaces
- Minimum development effort
 - Leverage existing functions in building new features

Minimize disruption and risk!

Platform vendor (Cisco)
Chip vendor (Barefoot)
Customer/open source/



Challenges

Do not break what works

- · Vendor data plane code is well tested
- ... and we don't want to need regression testing

Don't want to show, don't want to see

- · Vendor code and custom code may be confidential
- Not practical to familiarize with a lot of vendor code to just write a few lines

Resource availability

• Still "limited" on current chips

Data/control plane dependence

- Net OS should keep working
- Net OS should not be aware of custom data plane functions

In a nutshell

P4 and its ecosystem were not designed for incremental programming





We need to explicitly support

Incremental Programming

How can we address these challenges?

Identify constraints on new code

Enforce those constraints on custom code

Challenges

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Data/control plane dependence

- NXOS should keep working
- NXOS should not be aware of custom data plane functions

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Do's and Don't's

- Do add new
 - · Headers, parsers, tables, actions
- Do not modify existing
 - · Headers, tables, actions
- Modify in a controlled way parsers and control flow



No API

changes

NetOS

unaffecte

Customer Programming Workflow



daPIPE Data Plane Incremental Programming Environment

				data Plane Incr	emental Programmir	ig Environment - daPIPE		+ _ 🗆 X
Ex	it New	Save	Open	Set SDE path	Add/Update switch	Add/Update SDE build env	Clean database	View PD-API
P4 P	rogram TS	Swit	tchi	ng				
	Rename	_						
						v1 0 2		
					UdFIFE	V1.9.2		
			Add	Header/Register		Add A	ction/Table	
				Add Parser		Add Con	trol/Blackbox	
				Compile		Switch	Management	
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Support developers and streamline their task (while enforcing constraints)

Components of the Solution





https://github.com/FOXNEOAdvancedTechnology/ts_switching_P4

Specification

- A switch shall forward packets based on the RTP timestamp they contain
- If sent to 239.1.1.1, change destination address to 239.3.3.3 when RTP timestamp is
 - Between 0 and 2
 - Between from 5 and F
- If sent to 239.2.2.2, change destination address to 239.3.3.3 when RTP timestamp is
 - Between 3 and 4





Incremental Programming Unique Advantage

- Leverage existing features
 - Protocol parsing up to UDP messages
 - · Layer 2-3 forwarding, including multicast packet forwarding
 - Multicast routing (offered by the operating system)
- Focus on new feature
 - Write just a few lines of P4 code and control code

daPIPE bonus feature: no need to deal with the complexity of pre-existing code

Development Workflow

- Browse available (stock) metadata
- Define custom headers and metadata
- Specify parser(s) and their hook(s) in existing (stock) parsers
- Define custom tables and actions
- Specify control flow
- Compile and load on chip
- Develop control plane functionalities

Main window

data Plane Incremental Programming Environment - daPIPE									
Exit	New	Save	Open	Set SDE path	Add/Update switch	Add/Update SDE build env	Clean database	View PD-API	
P4 Prog	gram T : Rename	S Sw	itchii	ng					
					daPIPE	v1.9.2			
			Add	Header/Register		Add Ac	tion/Table		
				Add Parser		Add Cont	trol/Blackbox		
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Discl	aimer								

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Existing header view

	main.py		•
Exit Set SDE path Add/Update switch Add/Update VM Clean database			
Image: state stat	Current Headers Header instances	Header fields/size version iN diffserv totalLen identification flags fragOffset tt protocol hdrChecksum srcAddr dstAddr	Field Size/Length 8
	User Defined Header	s	
Header types	Header instances	Header fields/size	Field Size/Length
	Defete entry	De ete entry]

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							main.py	-	↑ _ □ ×
Exit	Set SDE path	Add/Update switch	Add/Update VM	Clean database	Save	Open			
•]								
н	eader type	rto t							
	ander instance	rtp_t							
п	eader instance	rtp							
Fi	eld	CSRC_count							
Si	ze/Length	4							
In	stance Metadata								
	Delete	Add/Update							

Current Headers

Adding RTP header

Header types	Header instances	Header fields/size	Field Size/Lengt
acl_metadata_t	A		
egress_intrinsic_metadata_for_mirror_buffer_t			
egress_intrinsic_metadata_for_output_port_t	_		
egress_intrinsic_metadata_t			
egress metadata t			
erspan_header_t3_t			
ethernet_t			
fabric_header_cpu_t			
fabric_header_t			
fabric_neader_dimestamp_t	w		
	User Defined Header	S	
leader types	User Defined Header Header instances	S Header fields/size	Field Size/Lengt 2
leader types	User Defined Header Header instances	S Header fields/size padding extension	Field Size/Lengt 2
Header types	User Defined Header Header instances	S Header fields/size padding extension version	Field Size/Lengt 2
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Header types	User Defined Header Header instances	S Header fields/size padding extension version	Field Size/Lengt 2
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Header types	User Defined Header Header instances	S Header fields/size padding extension version	Field Size/Lengt 2
Header types	User Defined Header Header instances rtp	S Header fields/size padding extension version	Field Size/Lengt 2
Header types	User Defined Header Header instances rtp Delete entry	S Header fields/size padding extension version Delete entry	Field Size/Lengt 2
Header types	User Defined Header Header instances rtp	S Header fields/size padding extension version Delete entry	Field Size/Lengt



Adding RTP parser

Disclaimer

Resulting Parsing Code

```
header type ethernet t {
    fields {
        dstAddr : 48;
        srcAddr : 48;
        etherType : 16;
header ethernet t ethernet;
. . .
header type rtp t {
    fields {
        version : 2;
        padding : 1;
. . .
        sequence number : 16;
        timestamp : 32;
        SSRC : 32;
header rtp t rtp;
. . .
```

```
parser parse ethernet {
    extract(ethernet);
    return select(latest.etherType)
        ETHERTYPE IPV4 : parse ipv4;
        default: ingress;
parser parse udp {
    extract(udp);
    return parse rtp;
parser parse rtp {
    extract(rtp);
    return ingress;
```

Stock code

Custom code Autom. code

Add action



Adding a table

						татъру			
Exit	Set SDE path	Add/Update switch	Add/Update VM	Clean database	Save	Open			
_	_				_	Actions	Variables name	Fields	
6	New ac	tion name: 🔤	ke_video(dstIP)			Metadata Headers	variables name	Tiends	
D	odify_field(ipv4.d	IstAddr,dstIP); Add action				acl_metadata_t egress_intrinsic_metadata_for_output egress_intrinsic_metadata_for_output egress_intrinsic_metadata_t form_pars egress_metadata_t erspan_header_13_t ethermet_t fabric_header_cpu_t fabric_header_timestamp_t fabric_header_t fabric_headata_t fabric_payload_header_t genv_t global_config_metadata_t	*		
						Tables			
-	New tal	ble name: sche	dule_table			Available	Actions	User defined tables	
rea i act t siz	ads { pv4.dstAddr : ex tp.timestamp : r tions { ake_video; drop; e : 16384;	tact; range;				terminate_pw terminate_tunn terminat	hel_inner_ethernet_ipv4 hel_inner_ethernet_ipv6 hel_inner_ipv4 hel_inner_ipv6 hel_inner_ipv6 hel_inner_on_ip hass from_rid _bd_stats NS: IP)		
	Delete table	Add table							
Discl	aimer								

	Ingress Pipeline beginning	- Contro	ls Tab	les
	appiy(shedule_table)	egress ingress USER C	acl_st adjust adjust ucompu co	ats
L.		Add to pipeline	egress	s_vni

Exit Set SDE path Add/Update switch Add/Update VM Clean database Save Open

main.py

Define control flow

apply(shedule_table)		ingress USER Controls:	adjust_lkp_fields bd_flood capture_tstamp compute_ipv6_hashes compute_other_hashes compute_other_hashes compute_other_hashes cpu_packet_transform dmac drop_stats ecmp_group egress_bd_stats egress_outer_bd_map egress_port_mapping egress_pystem_acl access_ban_viabe
	Add to pipeline		egress_vlan_xlate egress_vni
Disclaimer			

Compile and upload to switch

	main.py								 >
Exit	Set SDE path	Add/Update switch	Add/Update VM	Clean database	Save	Open			
•									
	Swit	ch address	(
	51110	chi uuuress		-					
	Rem	ote compilat	ion	2					
	Rem	ote IP addre	ss						
	User	name	1						
	_								
	Pass	word	L						
Disch	aimer								
Discl	annen								

Control Plane and NetOS Support



Open Challenges

- On the customer side
 - Debugging
 - Access to the right level of knowledge on the stock P4 program
- On switching system vendor side
 - Support model
 - Troubleshooting issues
 - Identify whether related to stock code of customer code
- On programmable ASIC vendor side
 - Offer technical support directly to the end customer for chip/compiler related problems