MAY 18-20 2021 P4 Workshop

Hosted by ONF

PL2: Towards Predictable Low Latency in Rack-Scale Networks

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Rack-Scale Architecture

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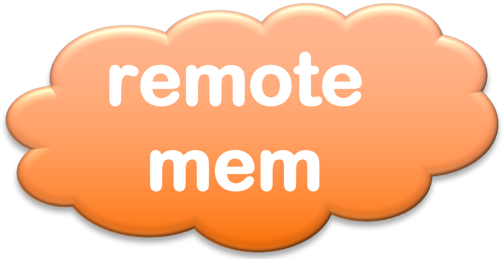

Rack-Scale Architecture

Intel® Rack Scale Design

NetCache

remote mem

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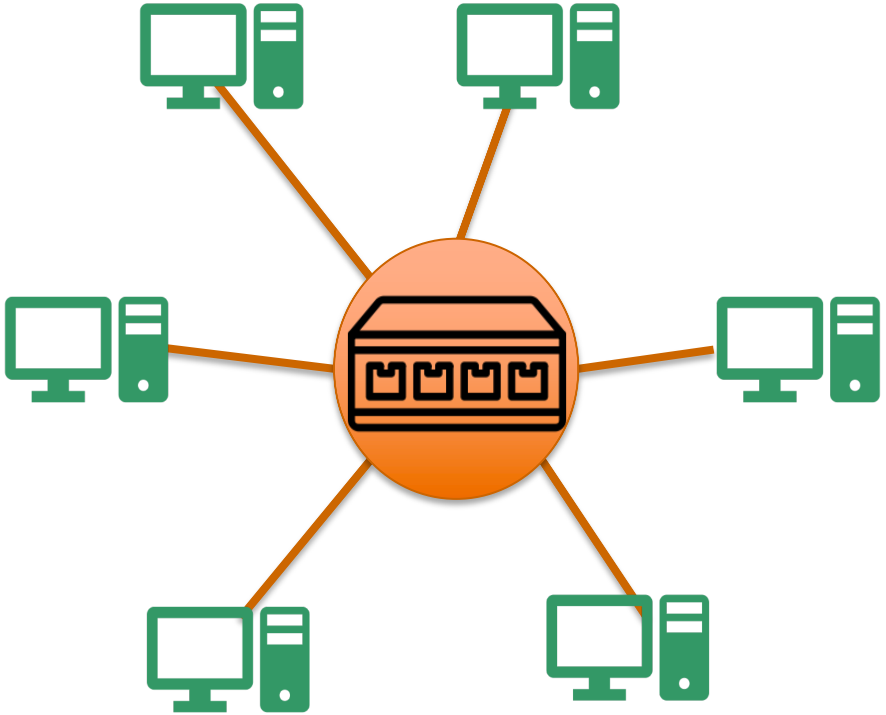

Motivation

- Network densities increases, switch buffer does not increase as fast
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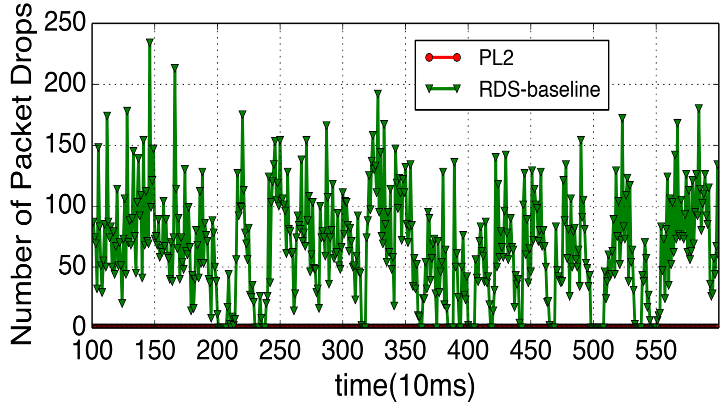
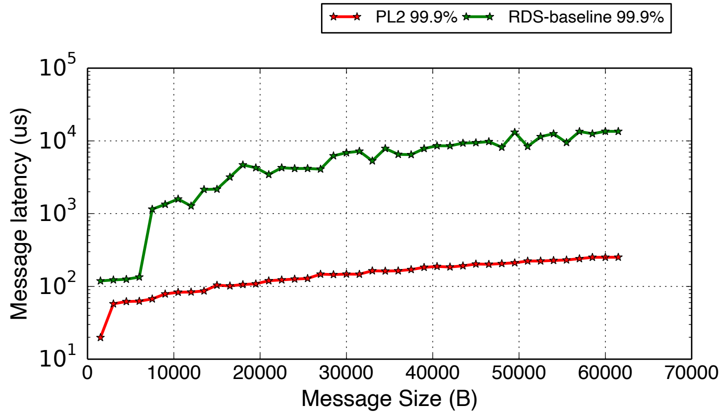
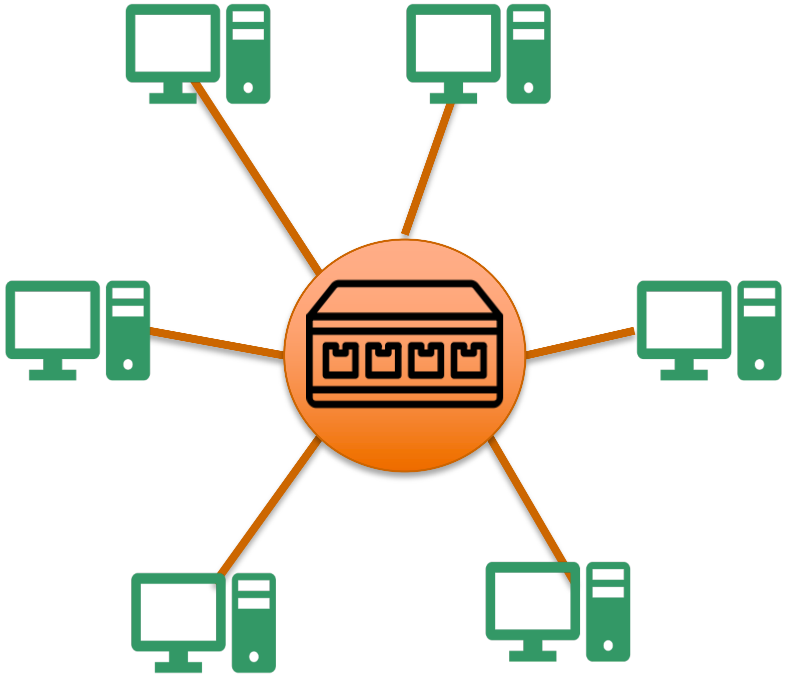




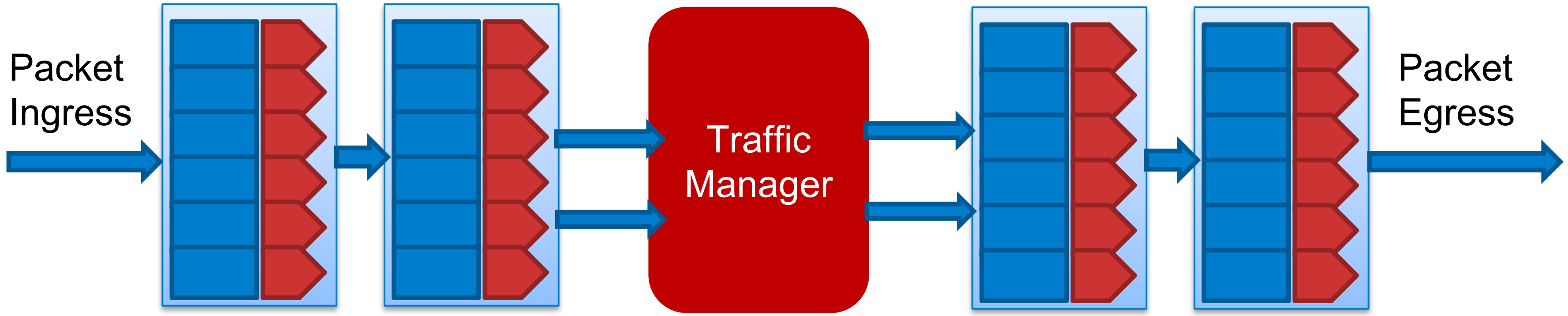
Architecture for Low Latency Network

- A single (ToR) switch to which all hosts are connected
  - Global knowledge of the demand
  - Global coordination across end-points



Programmable Switch

- Programmable switch offers in-transit packet processing and in-network state



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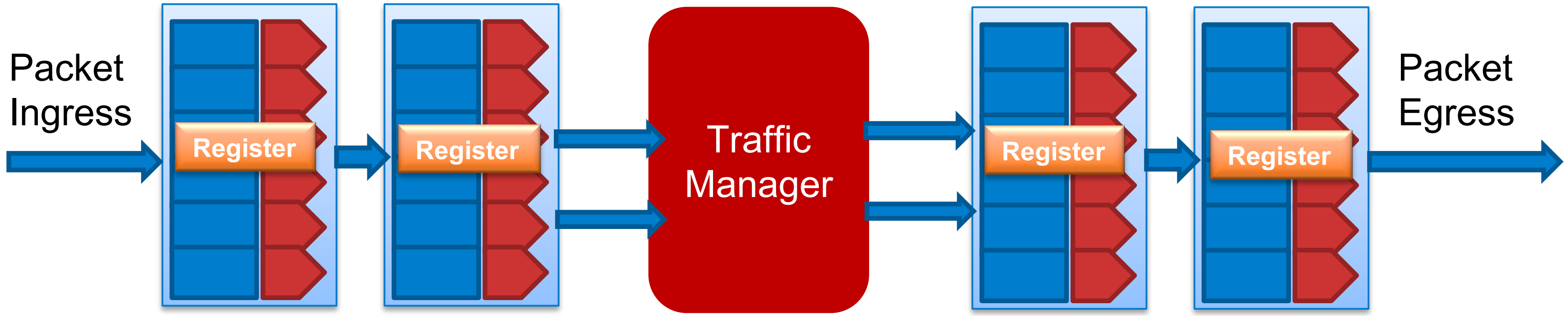

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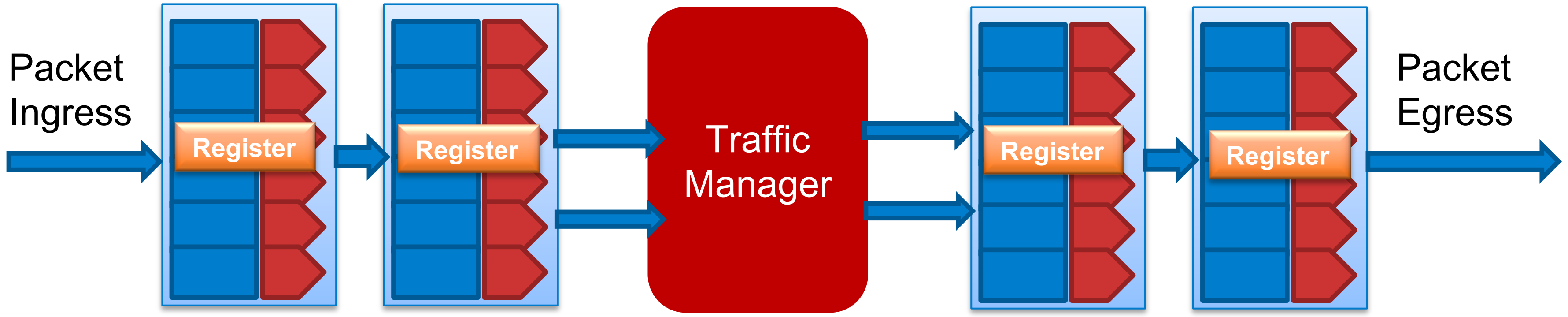
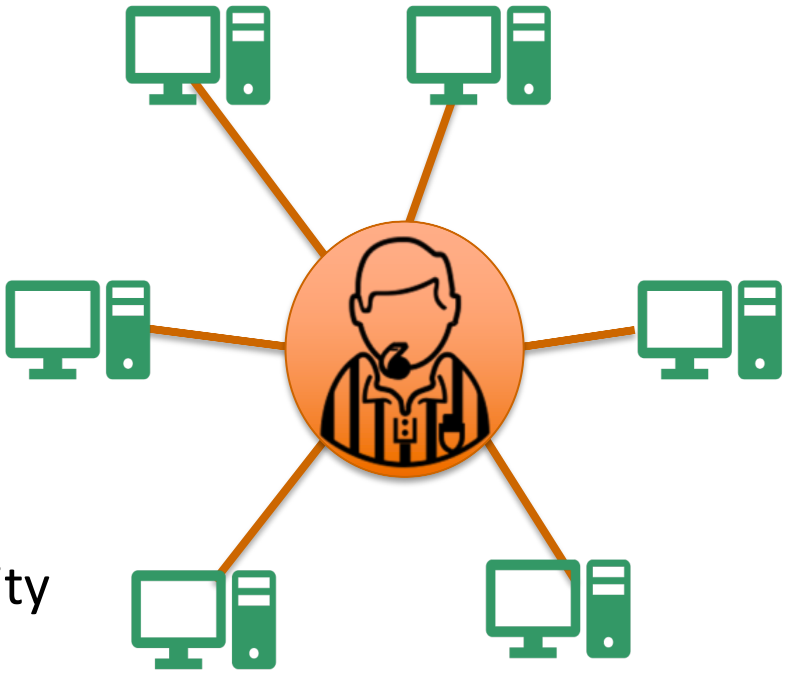


- Programmable switch as the centralized packet scheduler

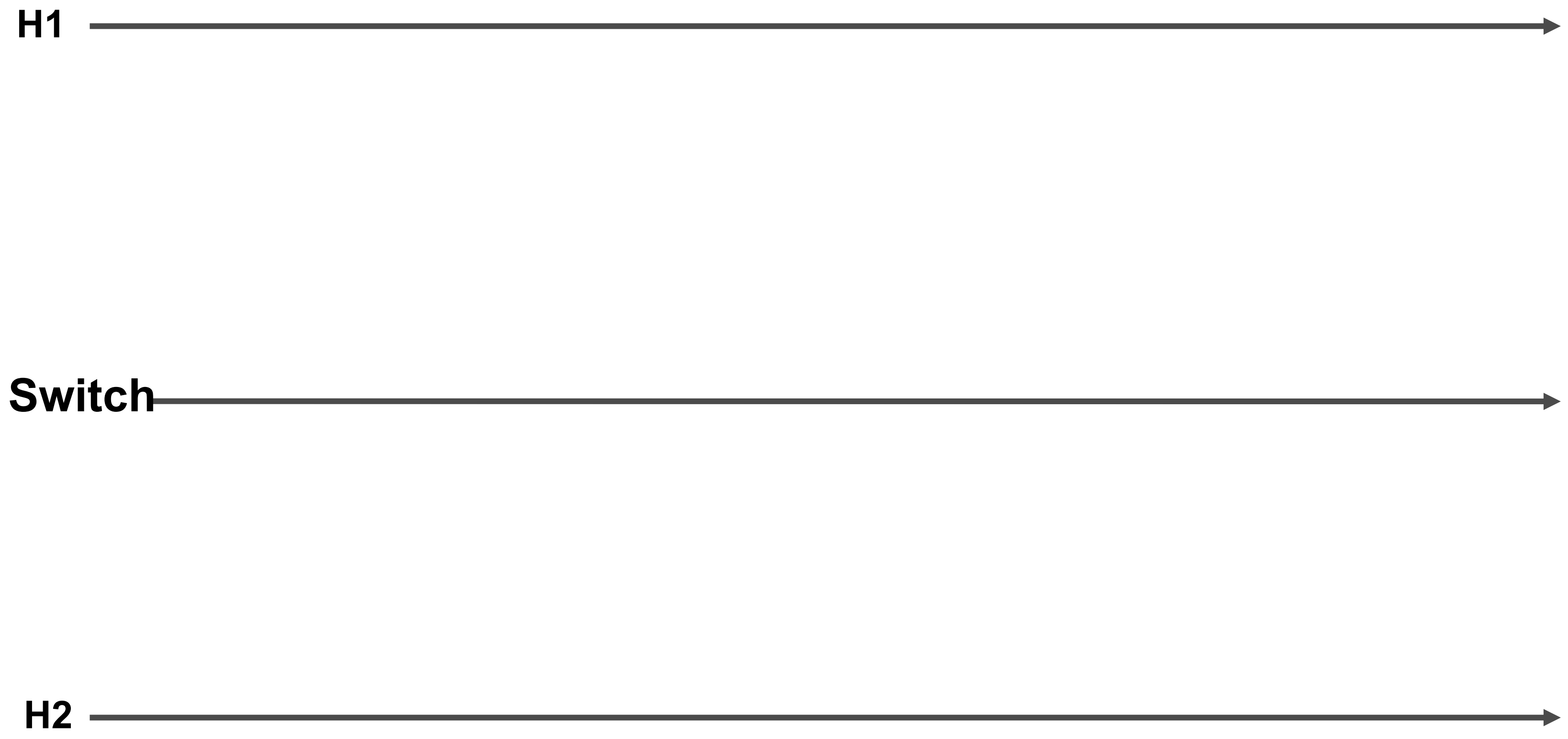
PL2: Centralized Scheduler

- Switch acts as an arbiter
  - Global visibility into packet reservation requests from all the endpoints
- Switch algorithm should fit
  - microseconds-level scheduling overhead
  - switch architecture, memory capacity
  - restricted programming model and memory access model



PL2 Overview

🟥 **Reserved timeslot** ☐ **Available timeslot**



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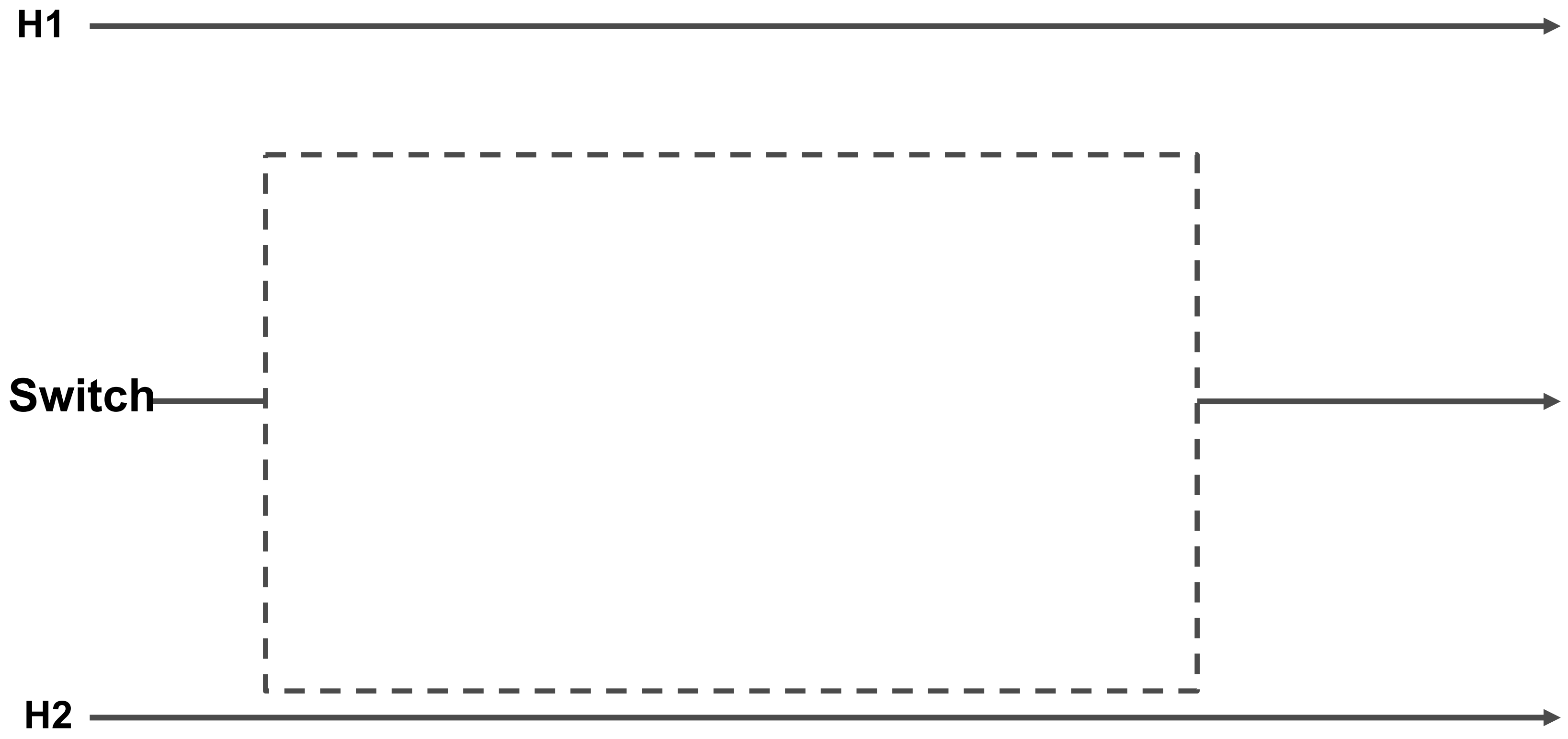

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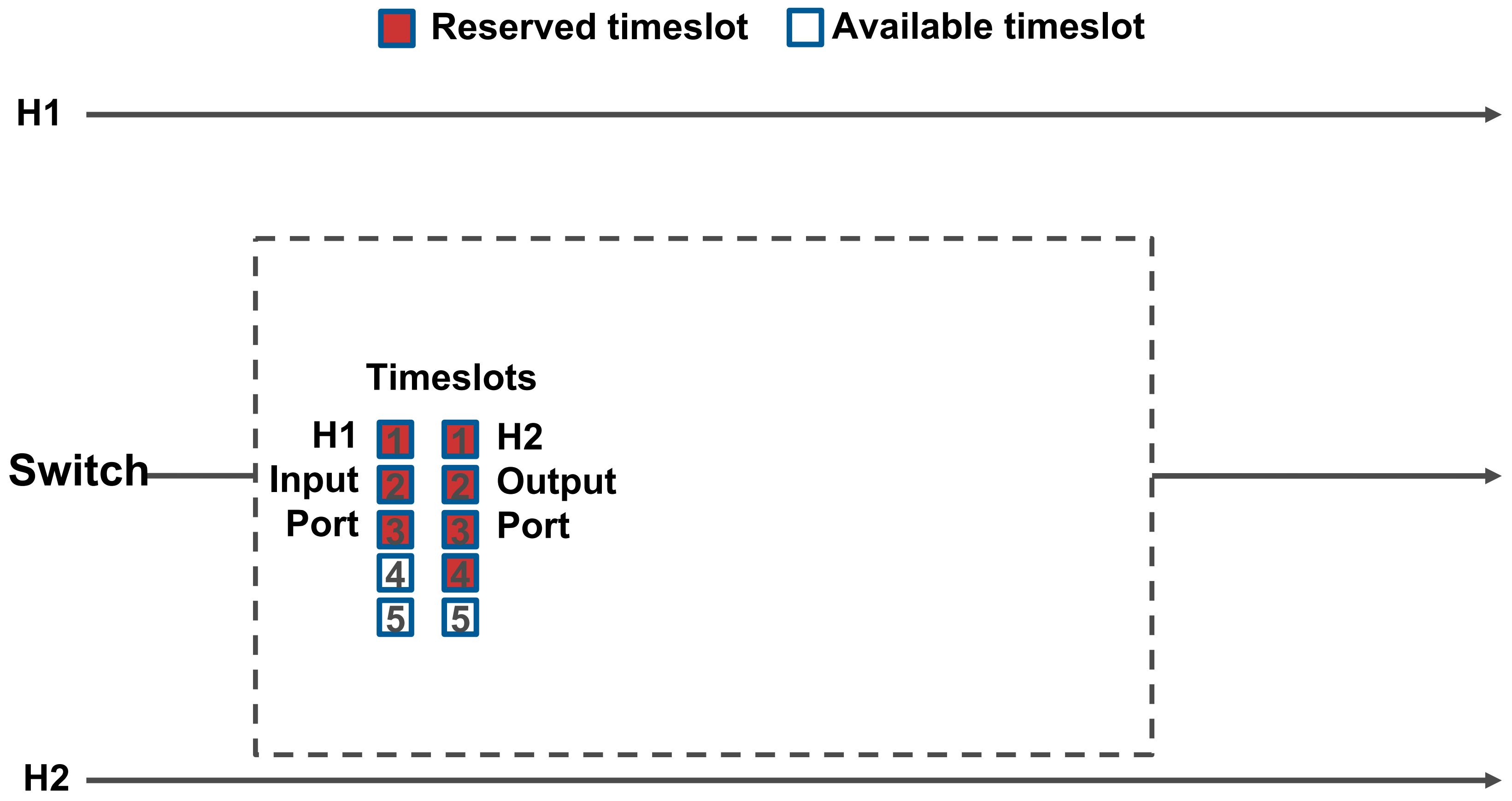

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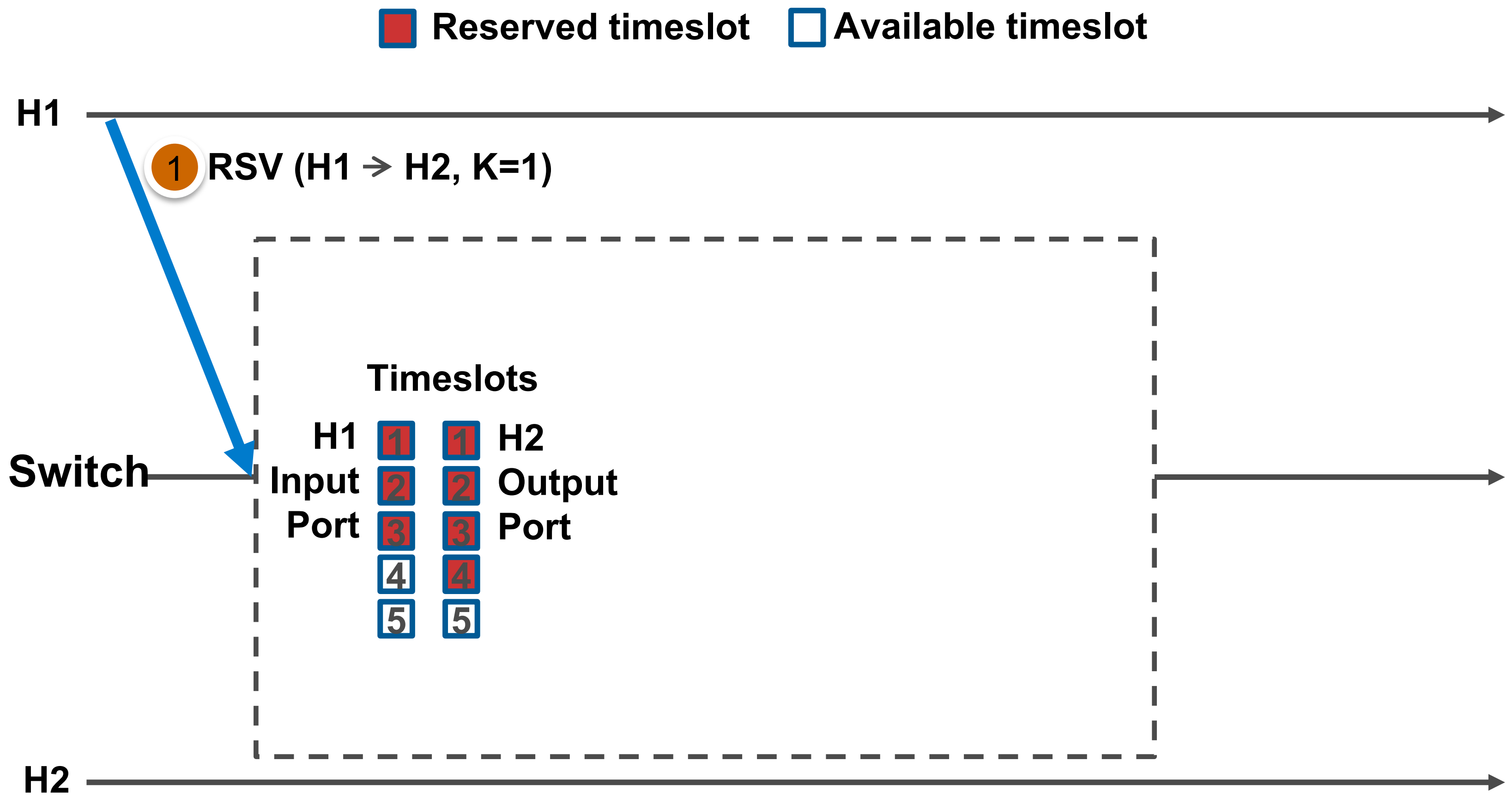

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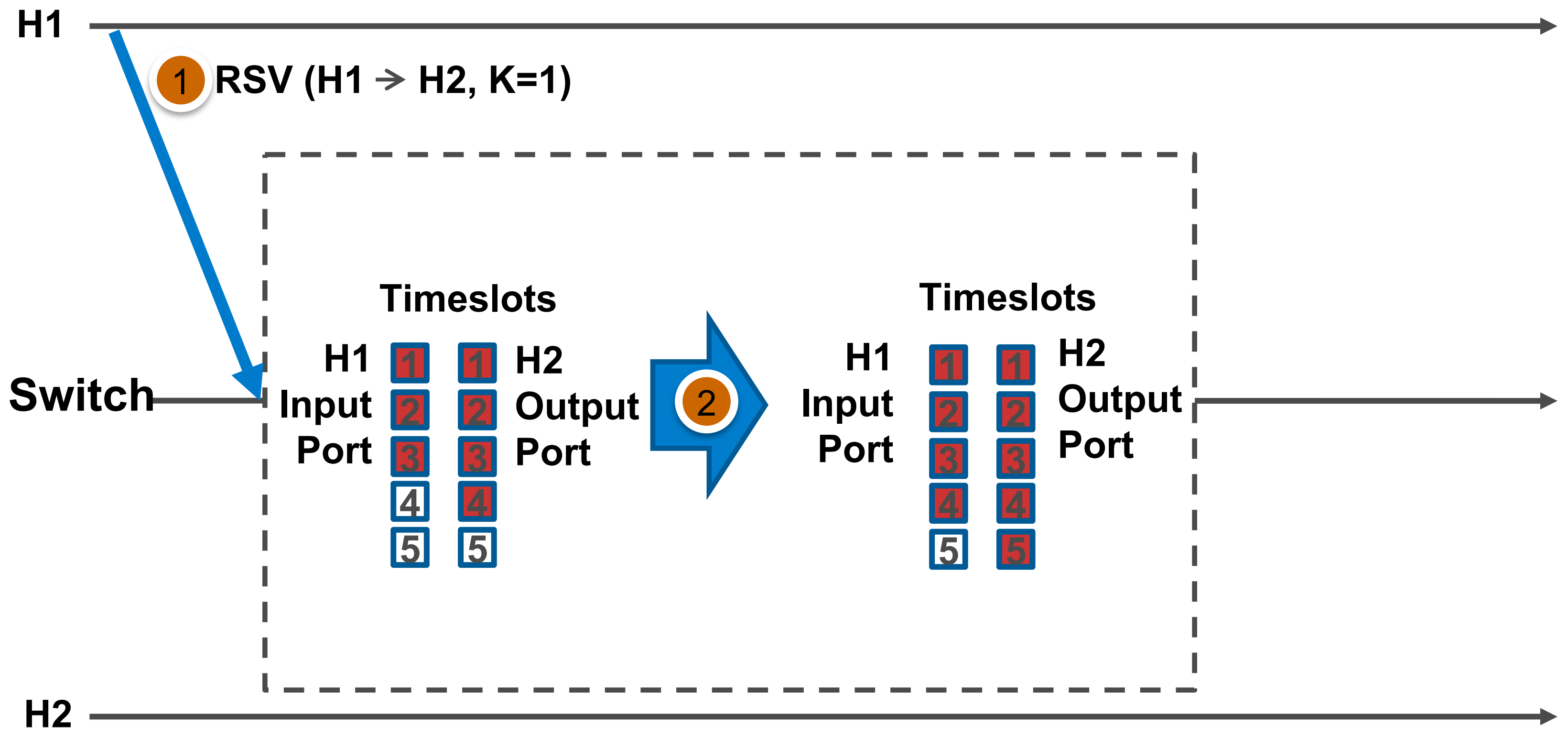

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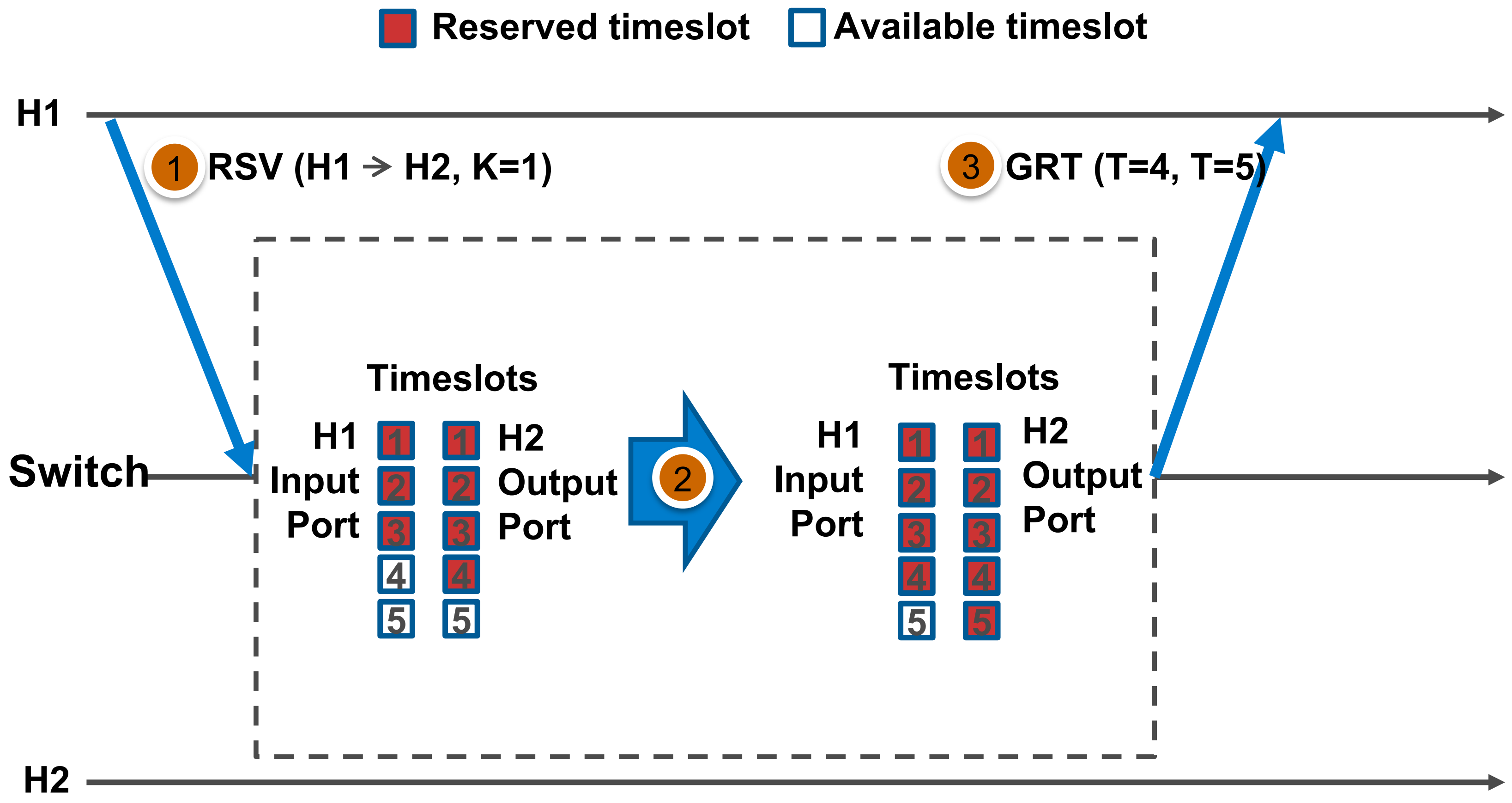

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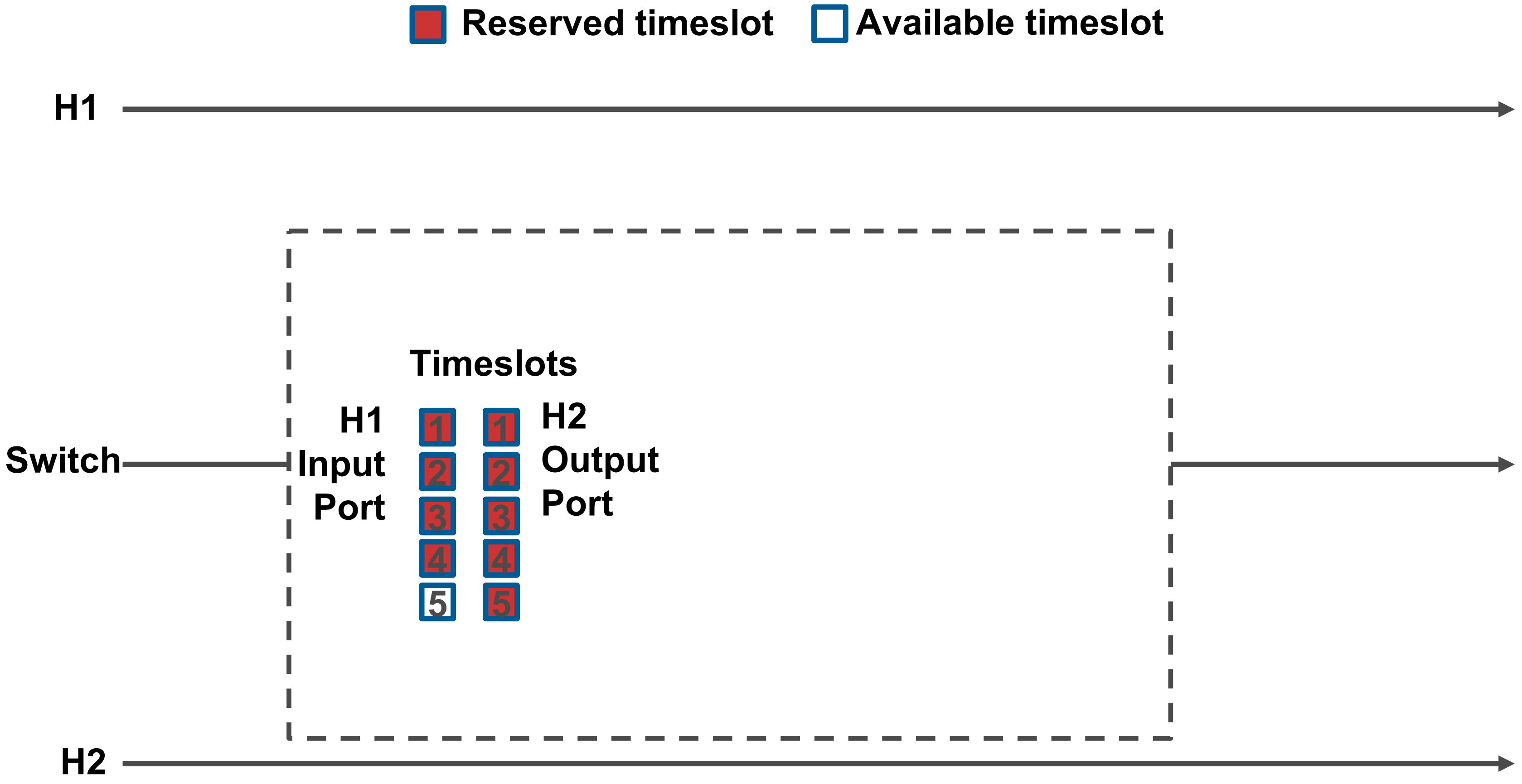

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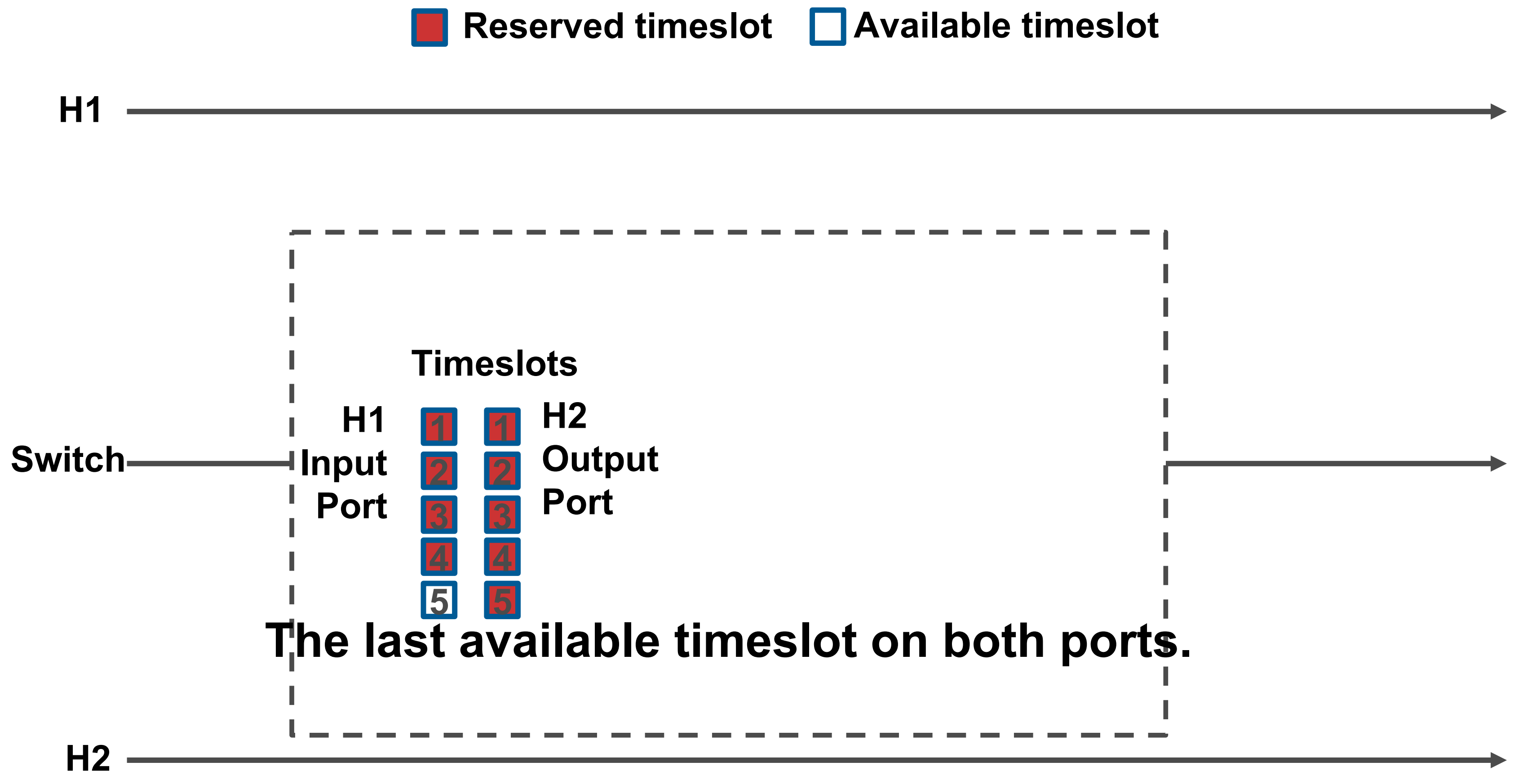

The last available timeslot on both ports.

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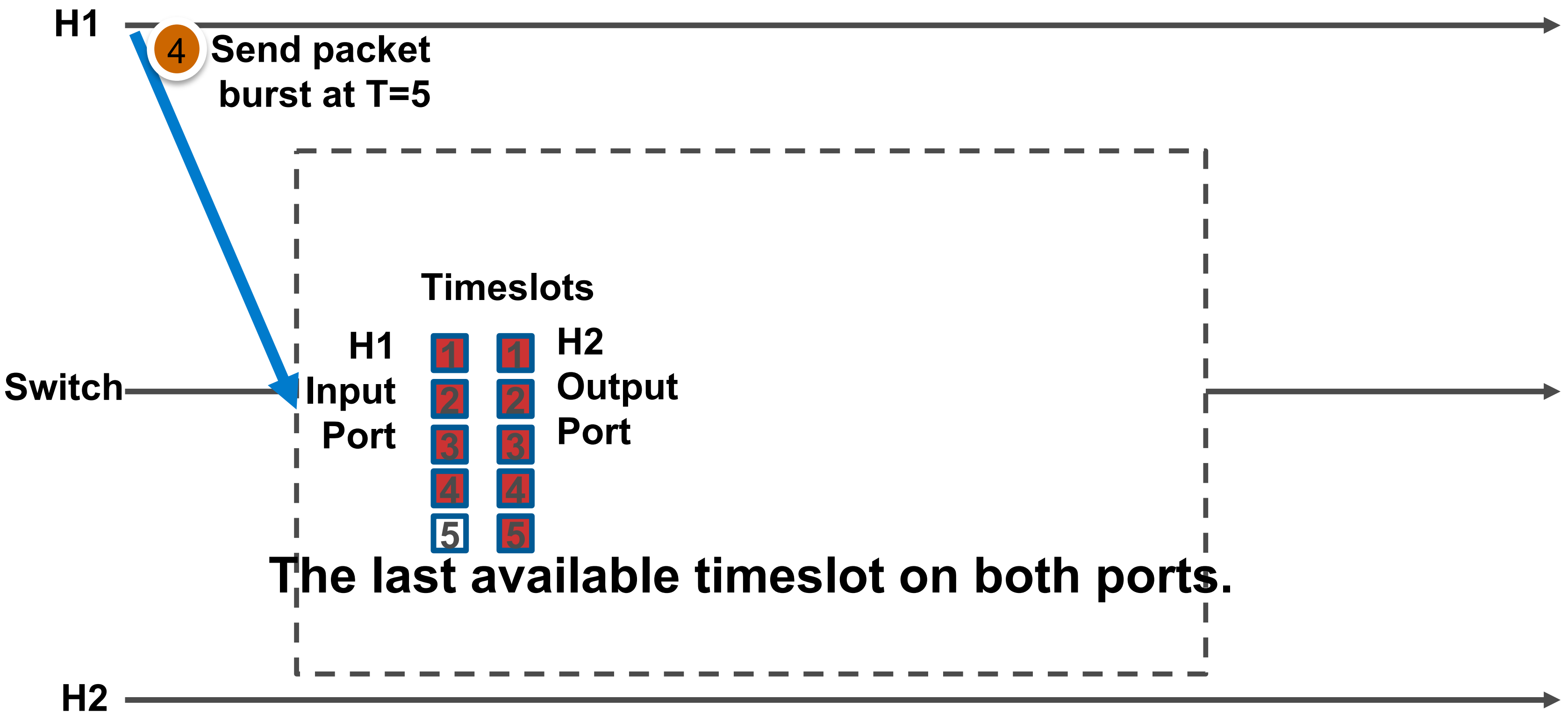

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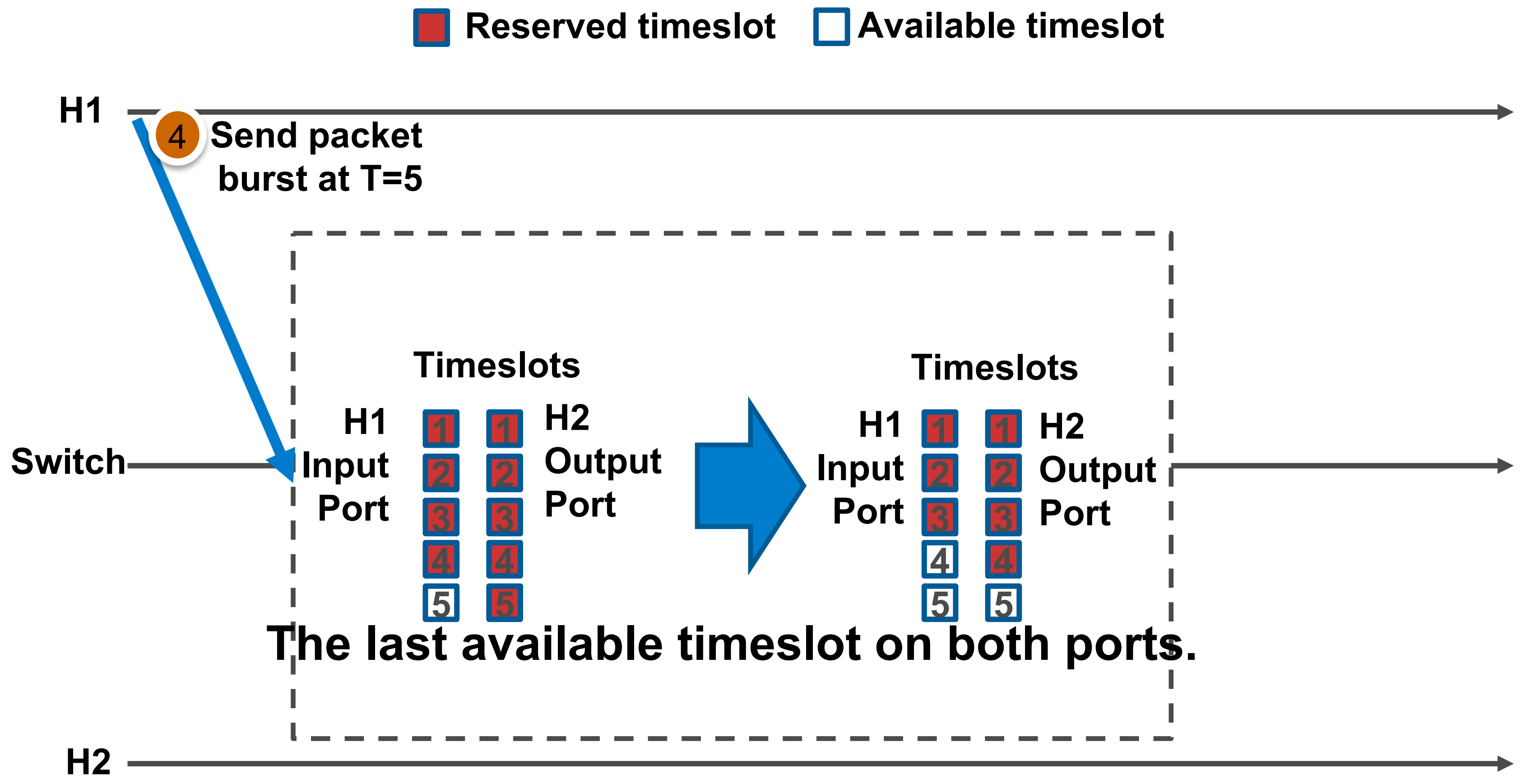

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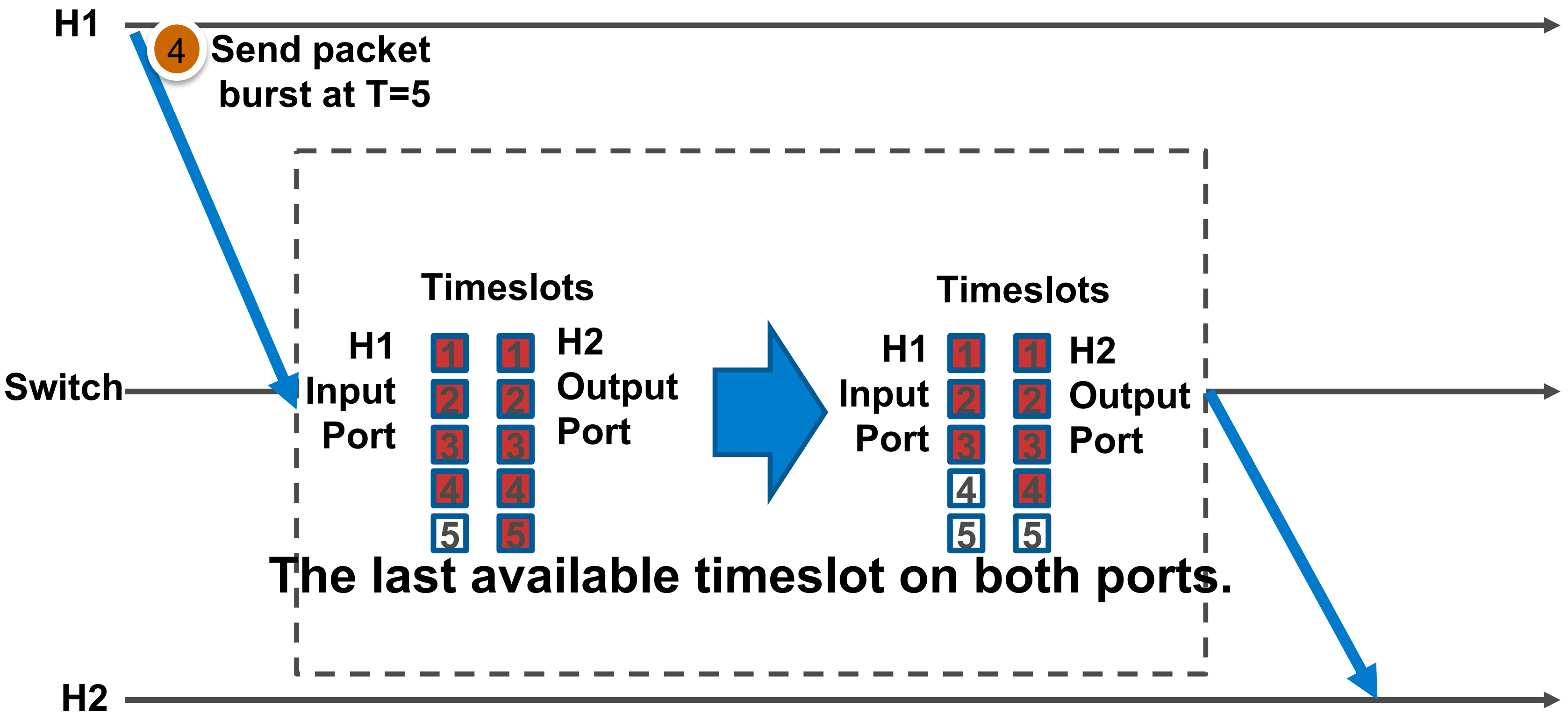

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Scheduling Overhead

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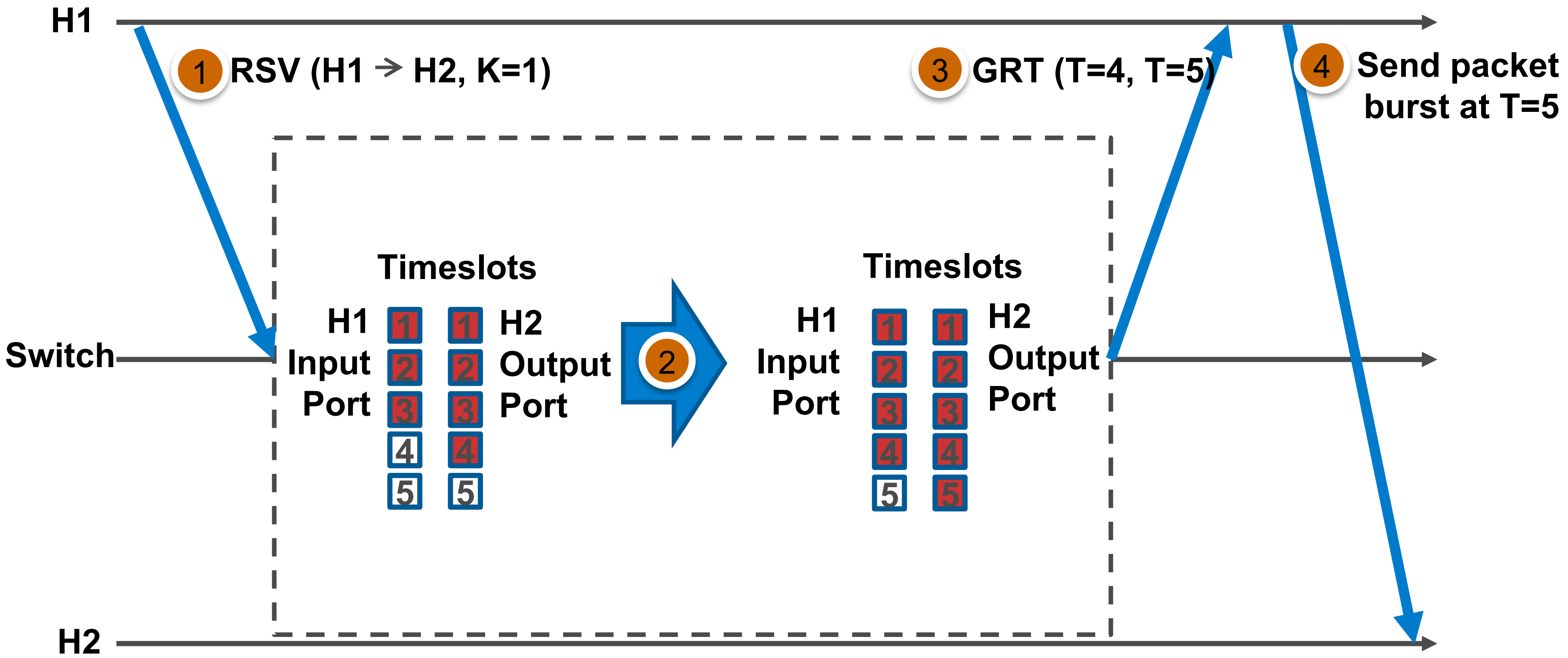

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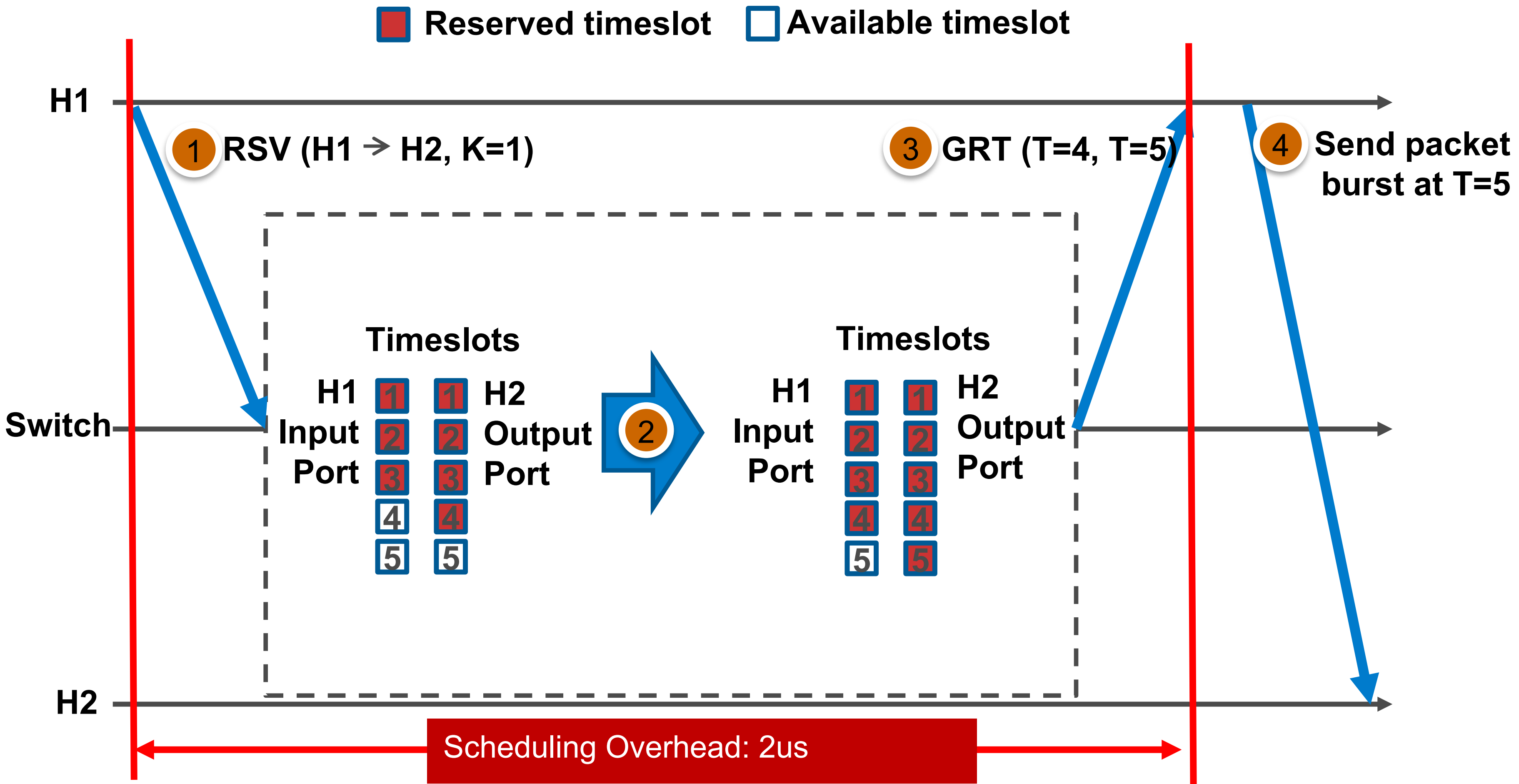

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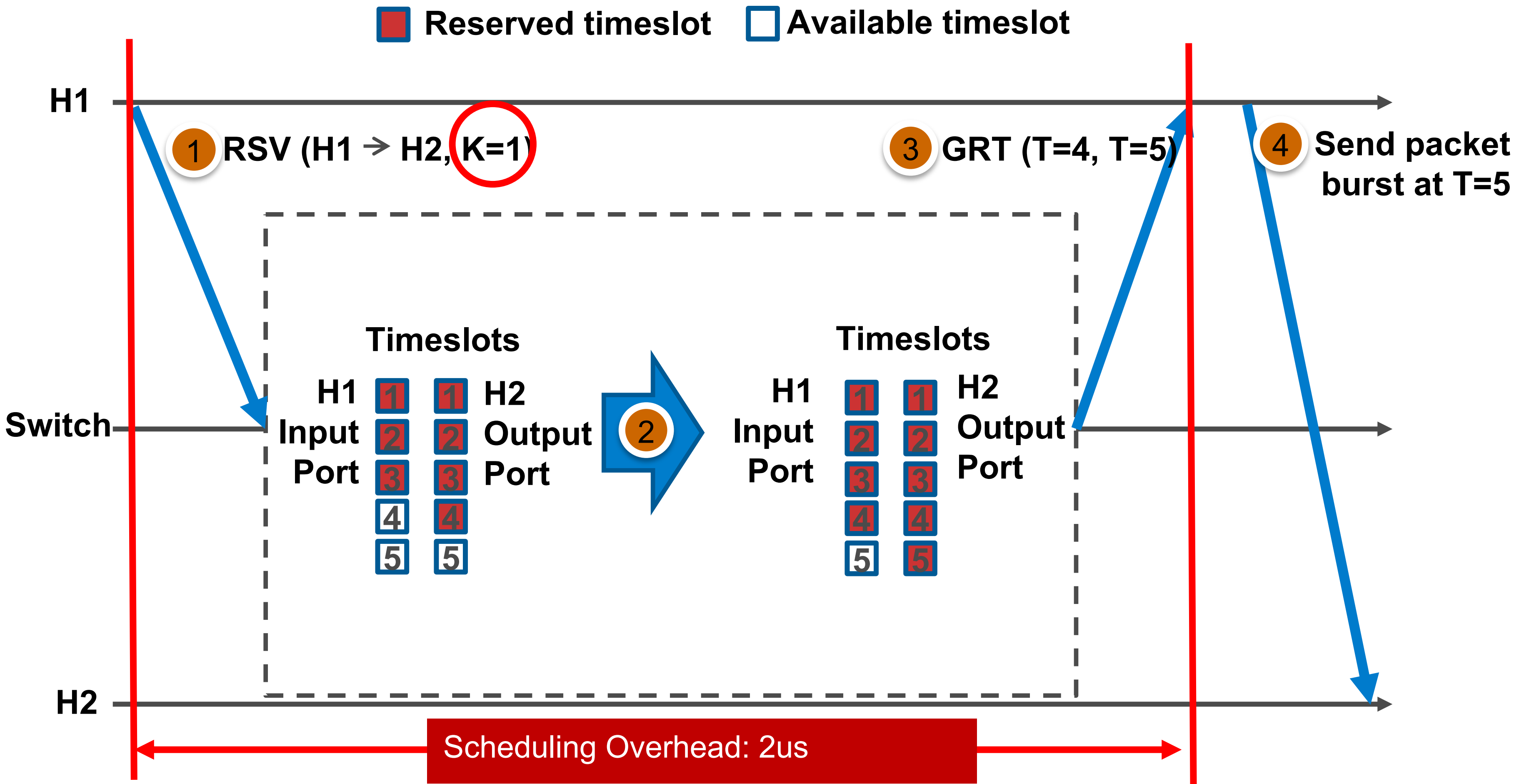

Scheduling Overhead

- Reduce the scheduling frequency, K=4
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End-to-end message latency is unbounded!

Prioritize Low Latency Message

- Switch grants a limited time slots (e.g., T2), for packets transmission

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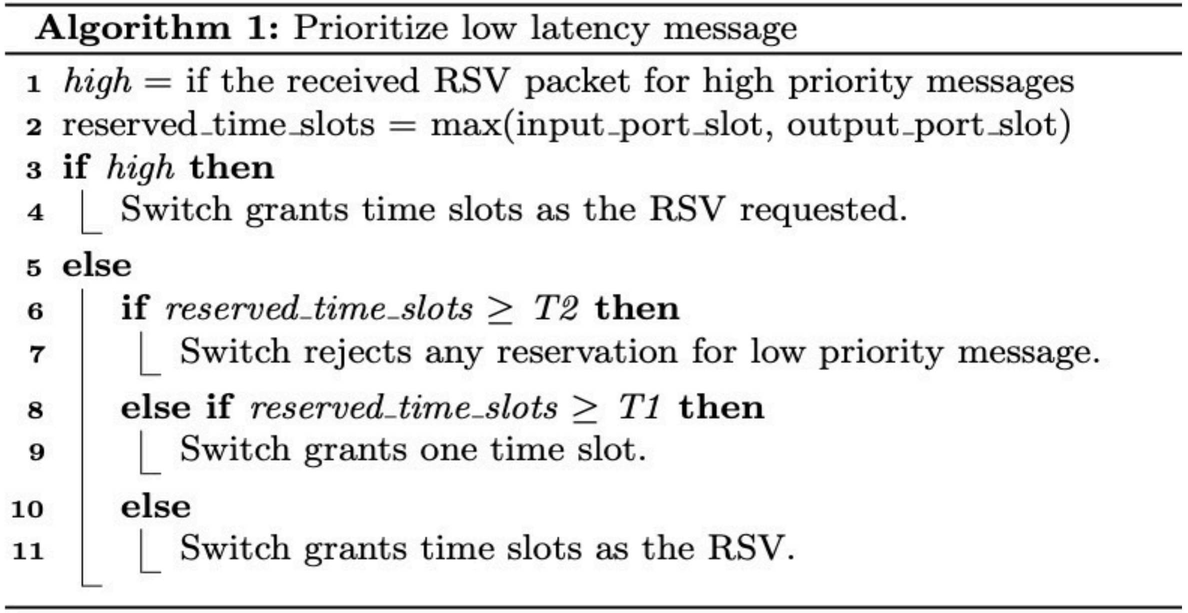
- Two properties
  - The maximum queue length is bounded by T2.
  - The `message` latency can be bounded by T2 + RSV-GRT-delay
    - When the network does not have more than T2 packets reservation from the high priority message
    - Set a bit for high priority message’s RSV packet

Prioritize Low Latency Message



Algorithm 1: Prioritize low latency message

```
high = if the received RSV packet for high priority messages
reserved_time_slots = max(input_port_slot, output_port_slot)
if high then
    Switch grants time slots as the RSV requested.
else
    if reserved_time_slots ≥ T2 then
        Switch rejects any reservation for low priority message.
    else if reserved_time_slots ≥ T1 then
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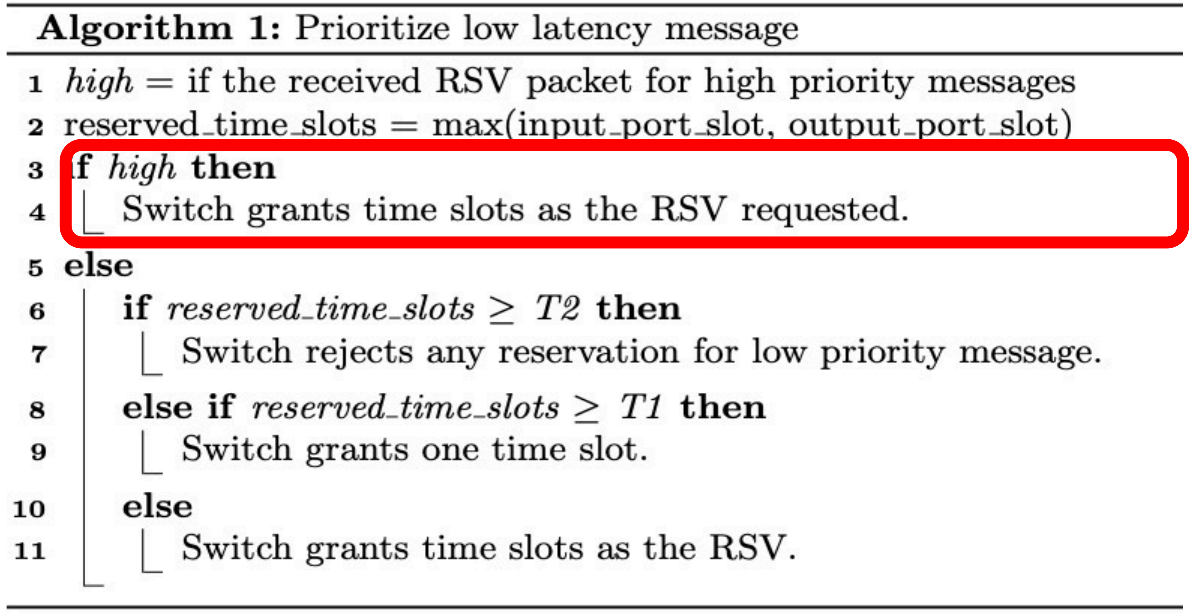
T1=64, T2 = 128

Prioritize Low Latency Message



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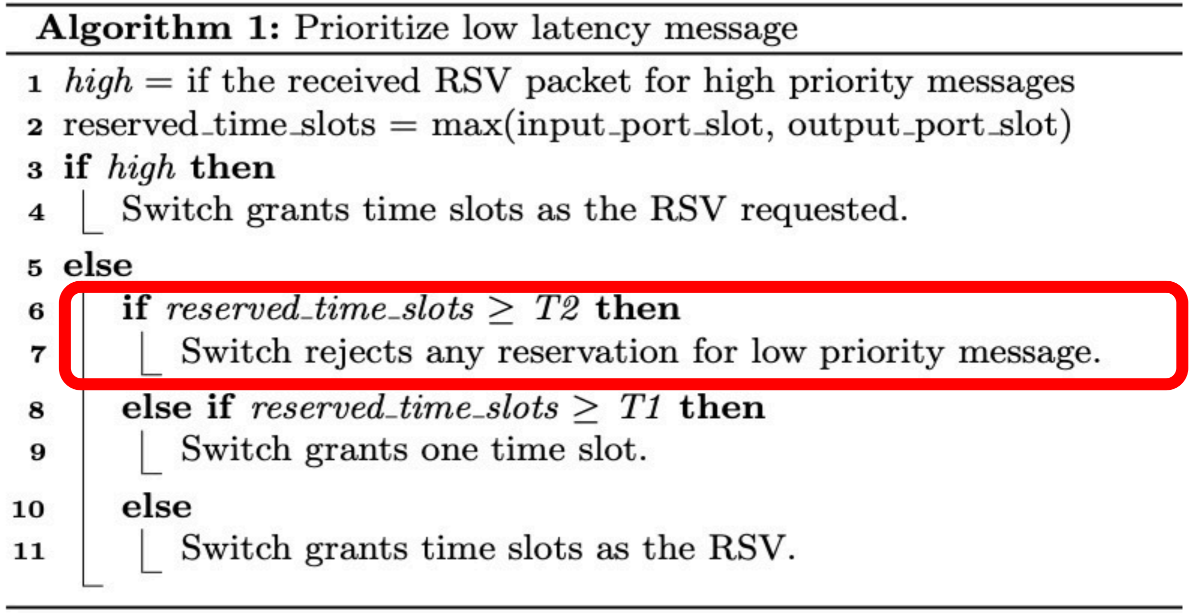

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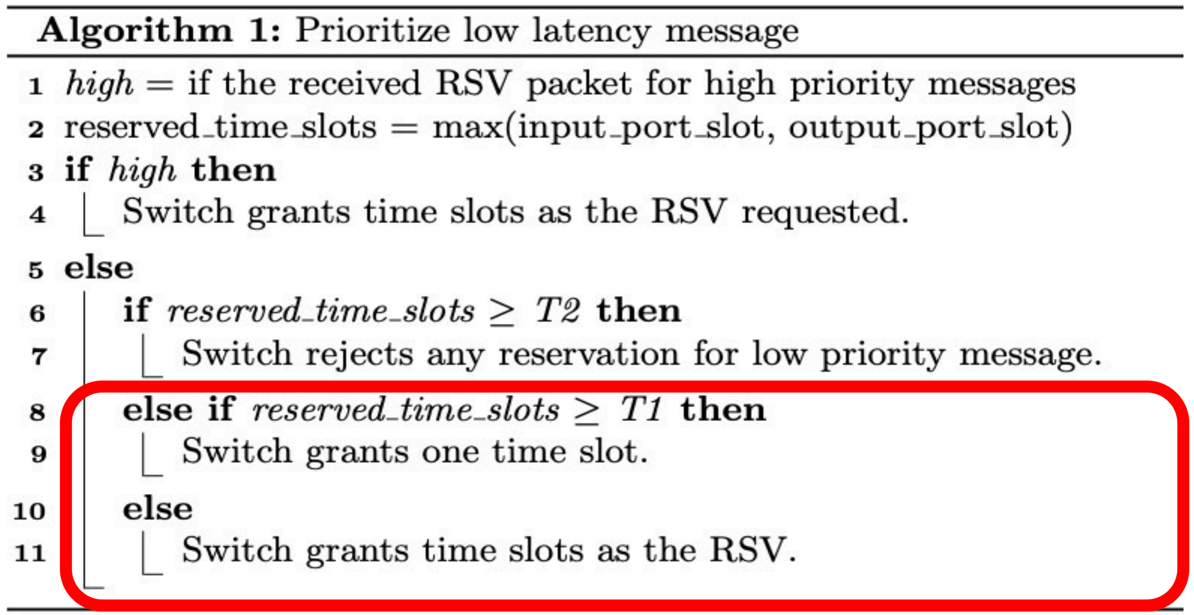

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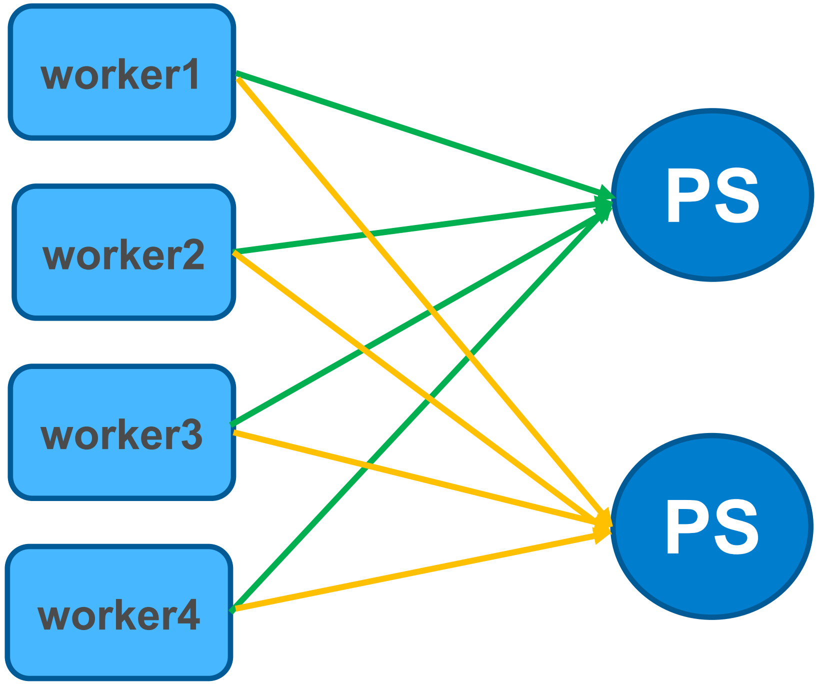
Implementation and Evaluation

- Implementation
  - A customized networking stack and Mellanox VMA, Userspace TCP stack
  - Use P4 to implement the centralized scheduling algorithm at Tofino switch
- Evaluation Setup
  - Testbed setup: 6 hosts connect to one Tofino switch
  - Baseline: Receiver-Driven Scheme (RDS); TCP+Cubic and UDP
  - Workloads: Memcached, VGG16, Workload trace (W1-W5) from Homa

PL2 v.s. RDS on VGG16



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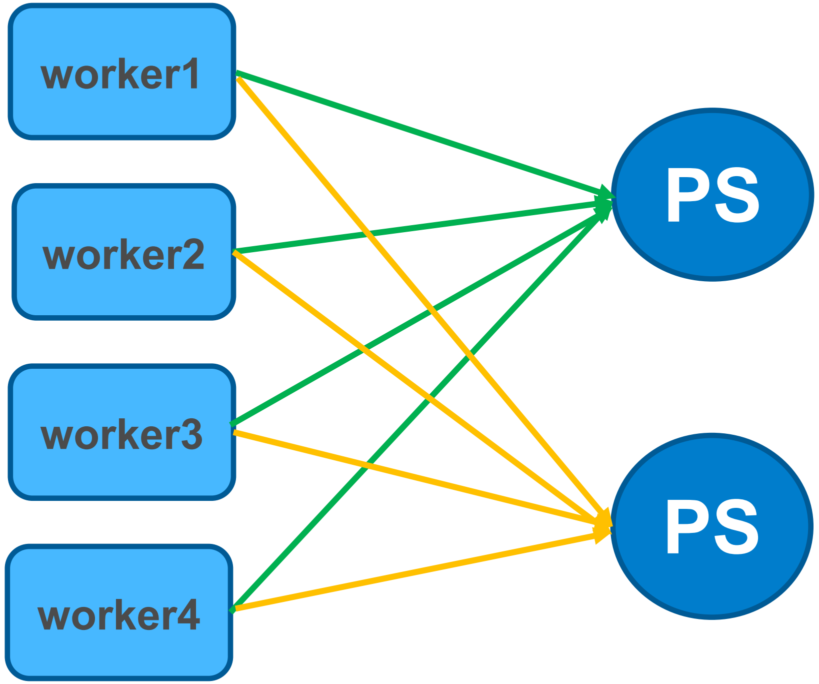

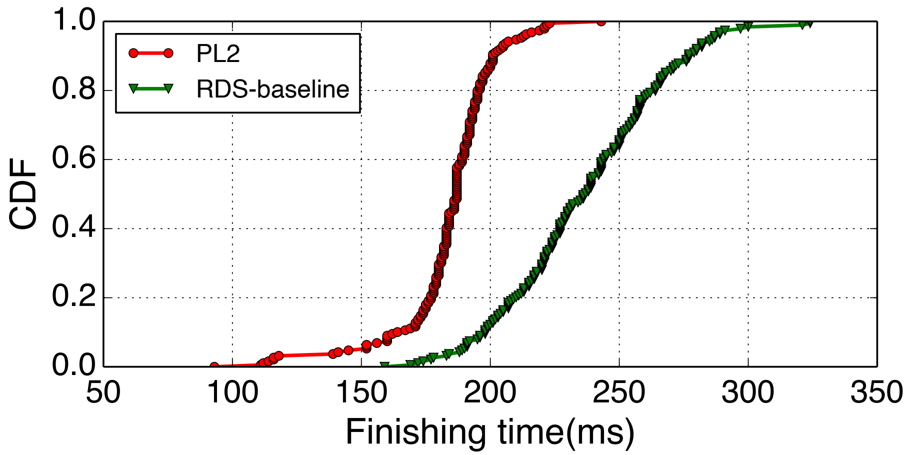

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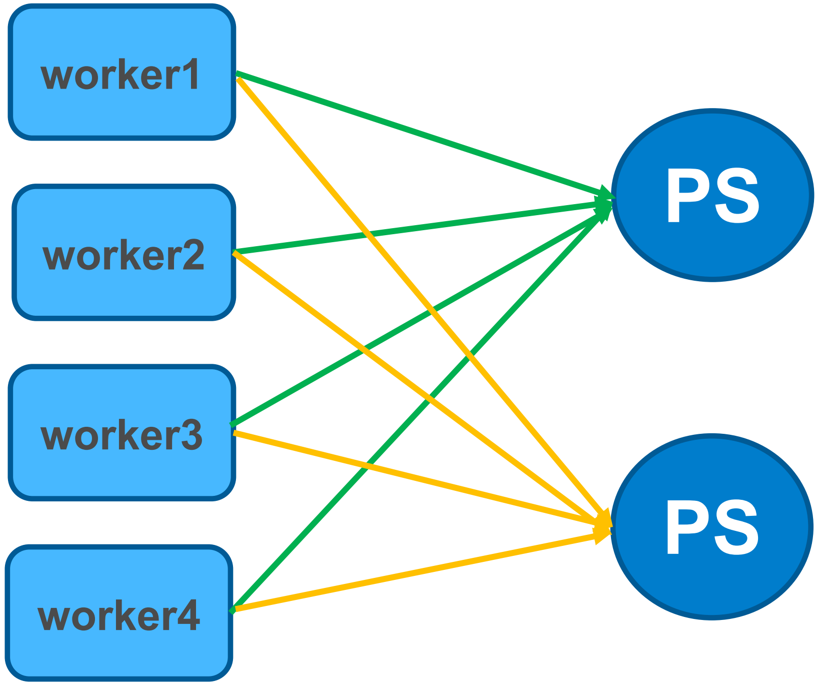
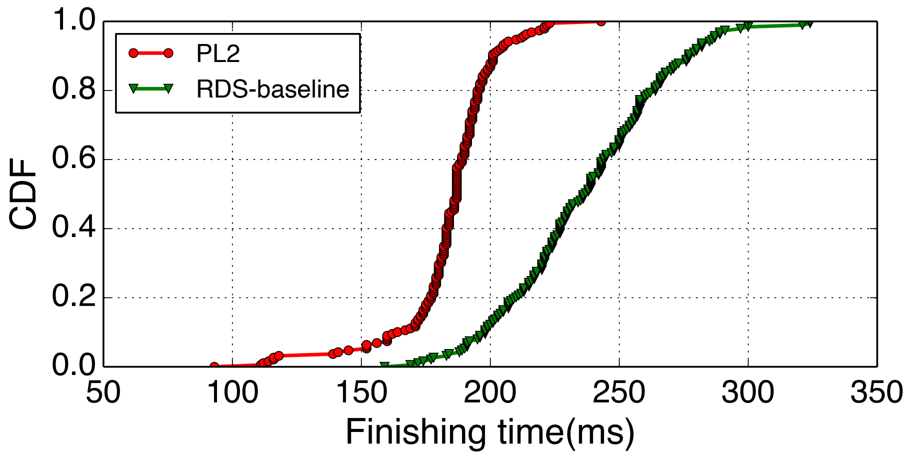
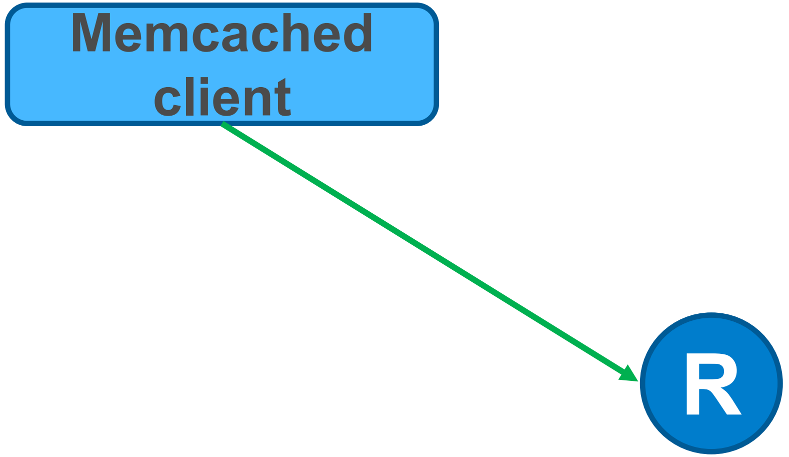
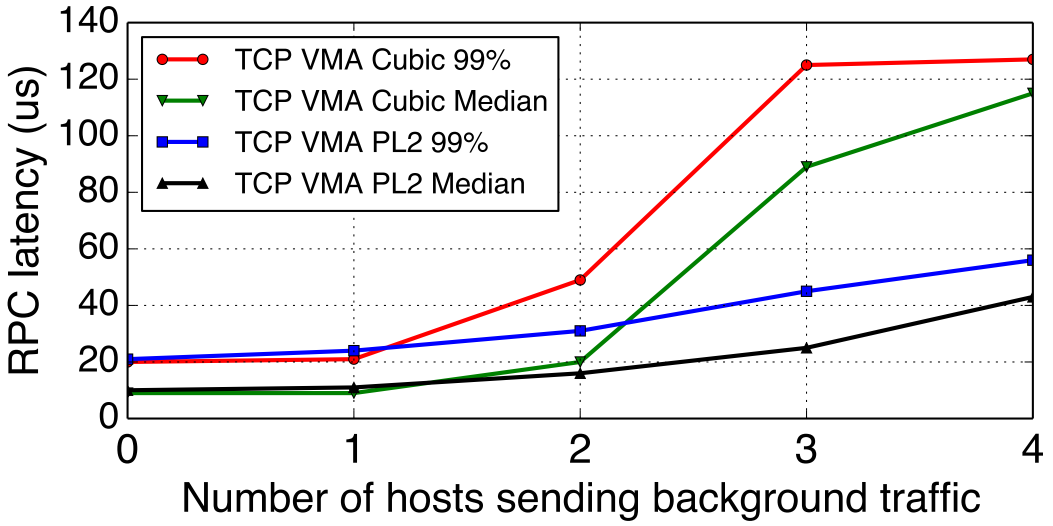




PL2 improves training latencies for VGG16 by 30%

Memcached competing Background traffic





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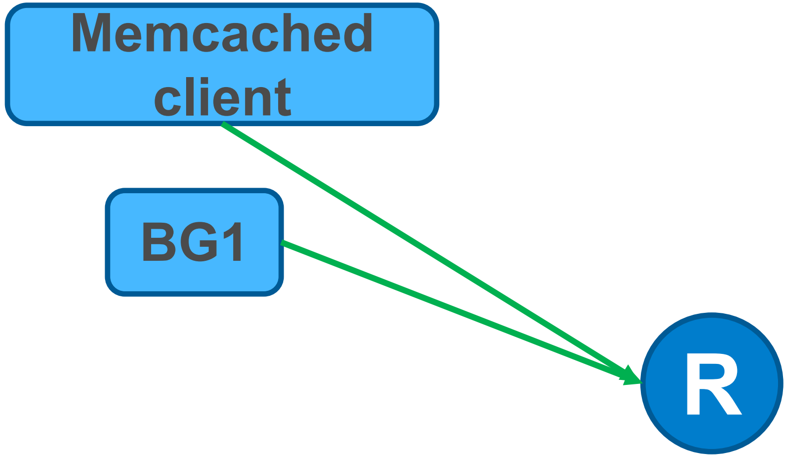

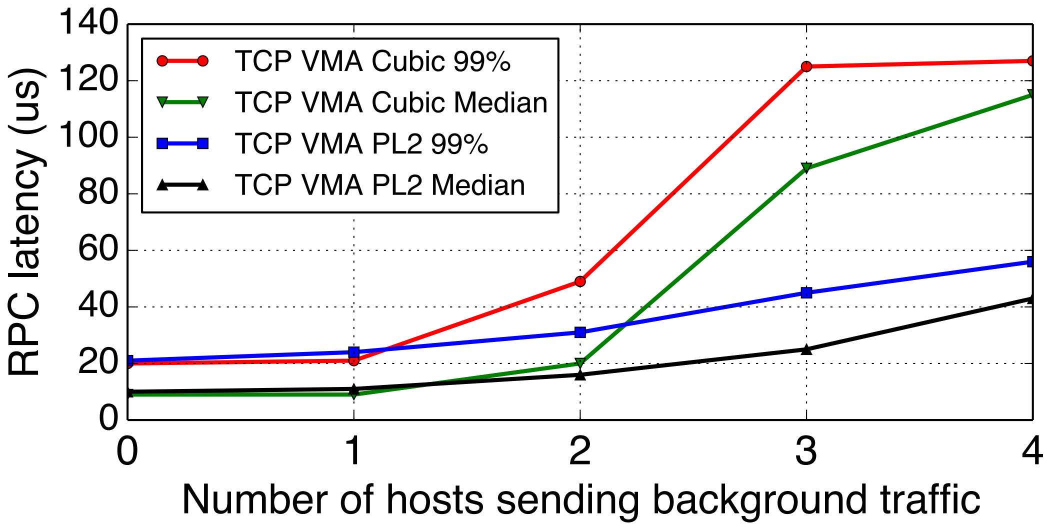

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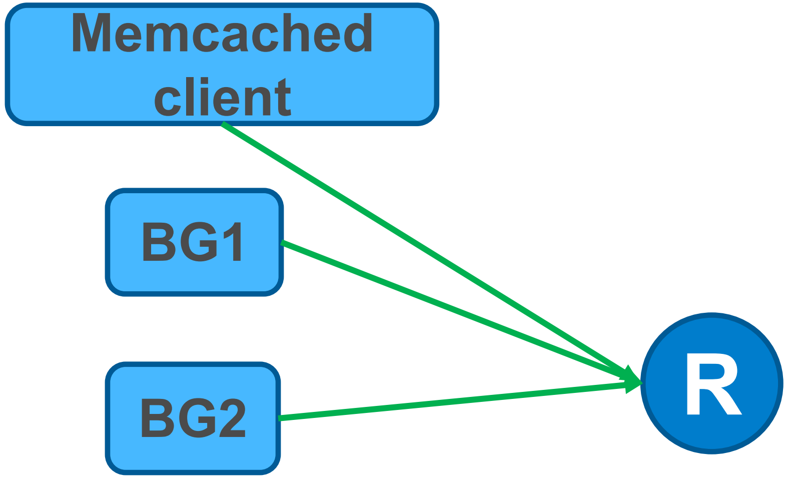

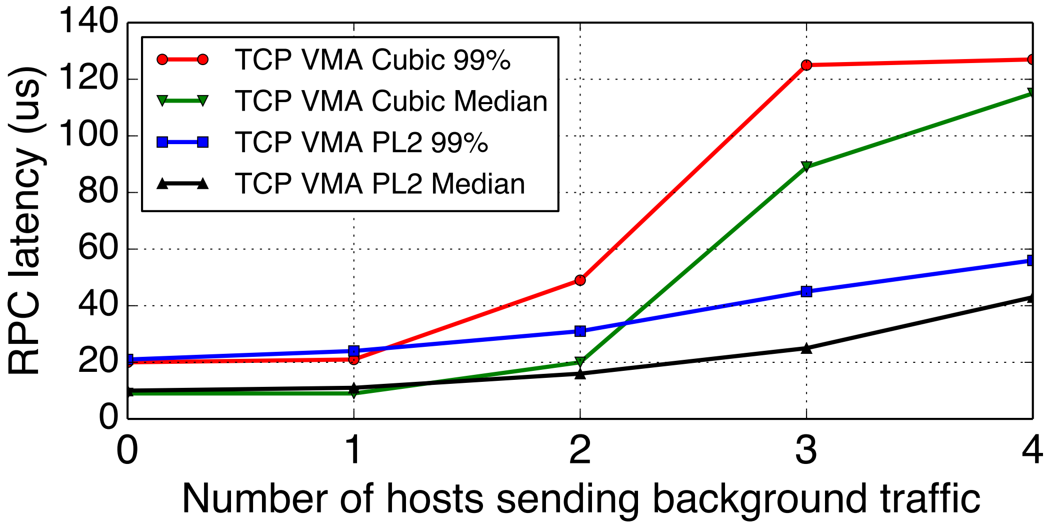

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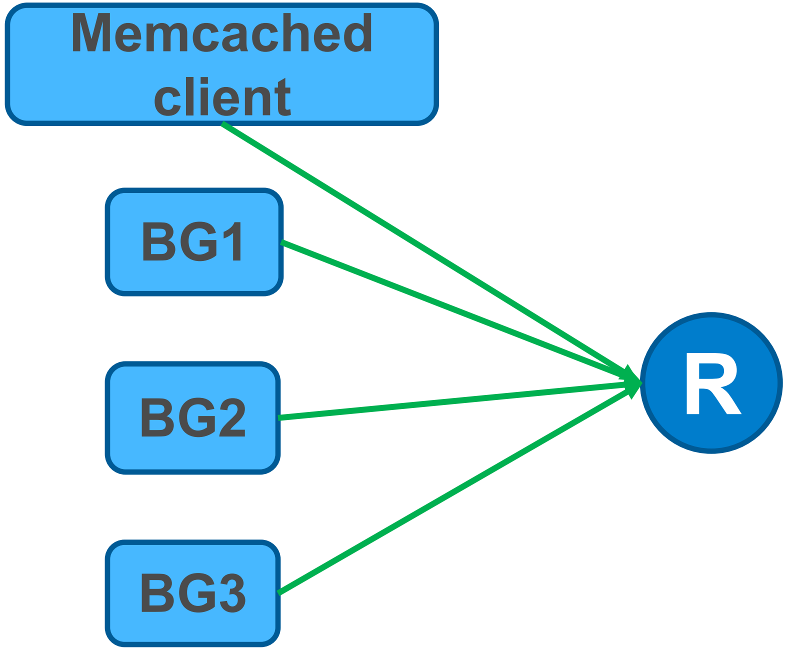

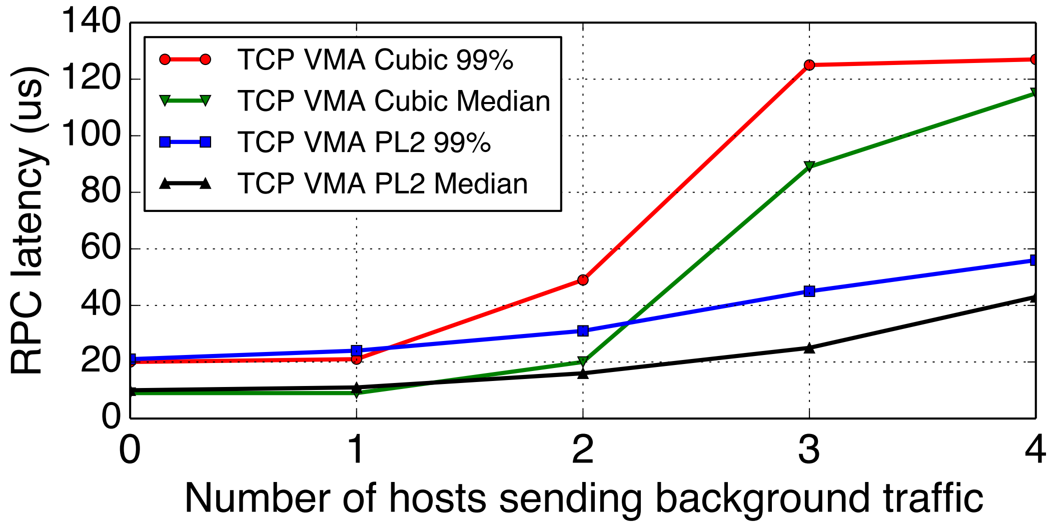

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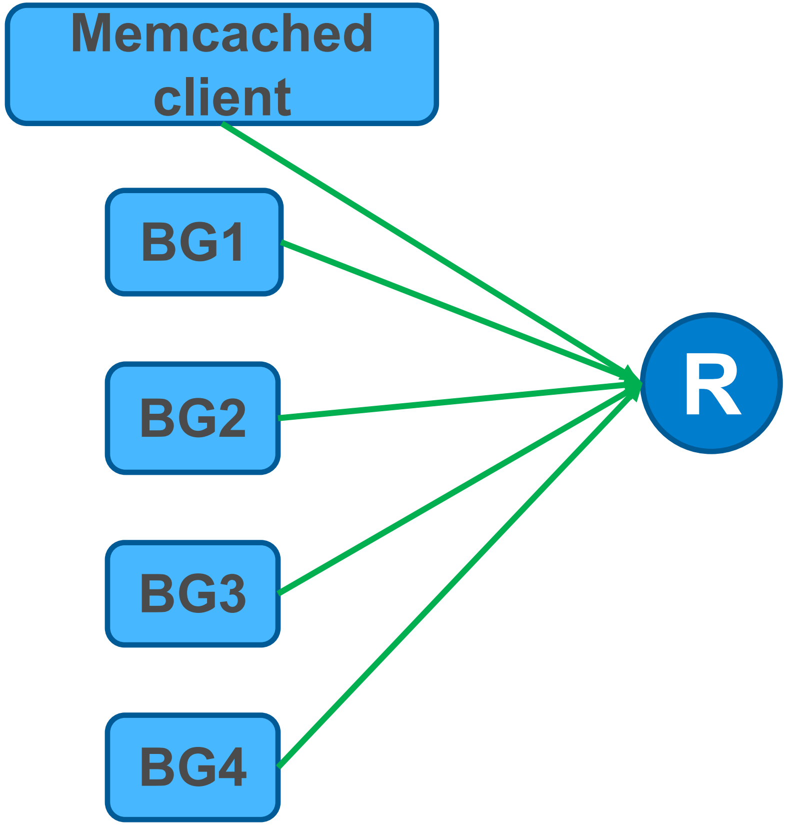

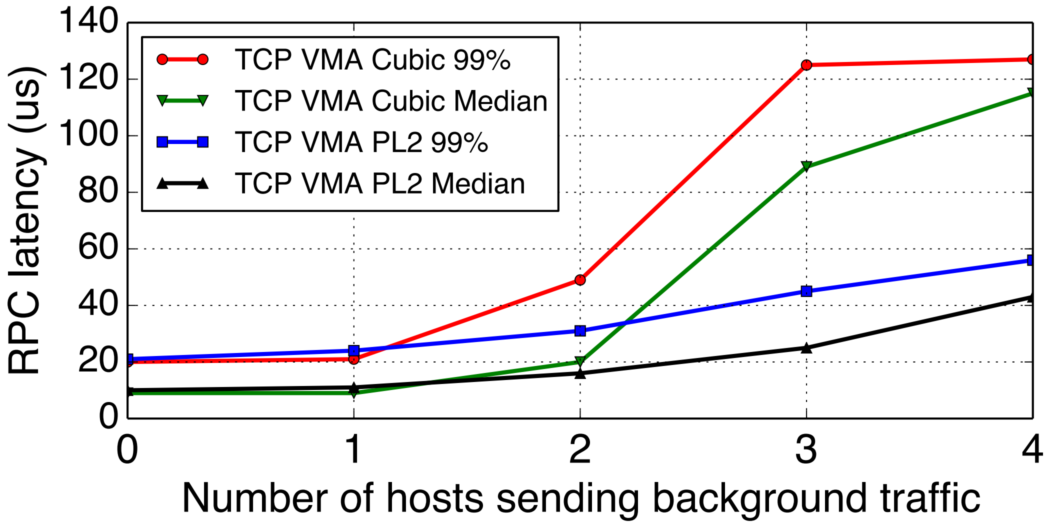

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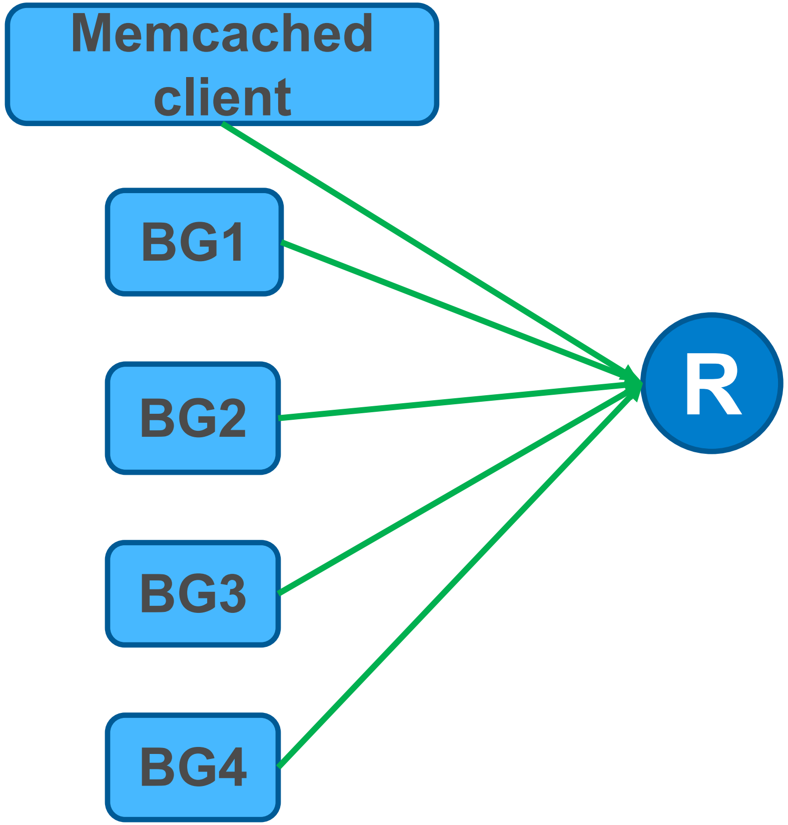

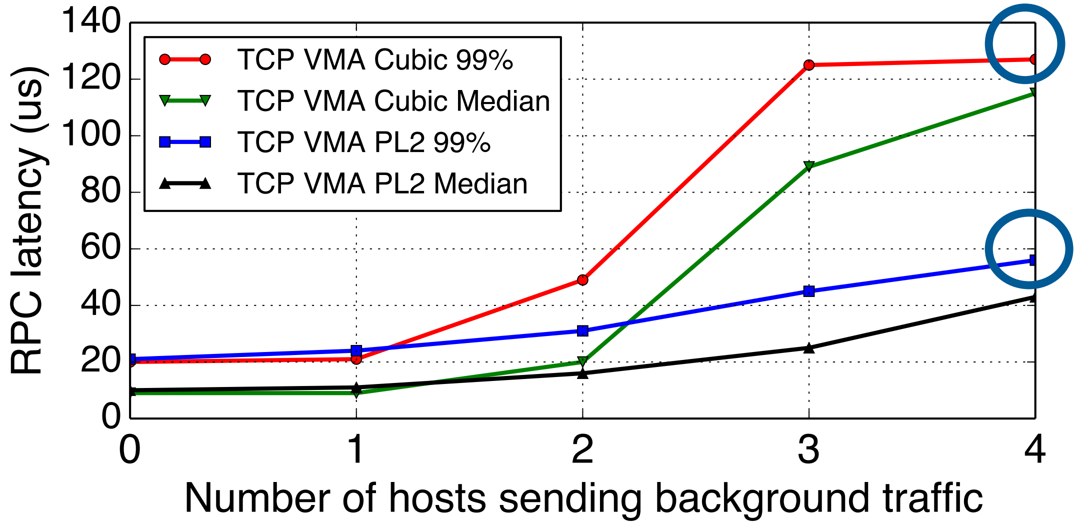

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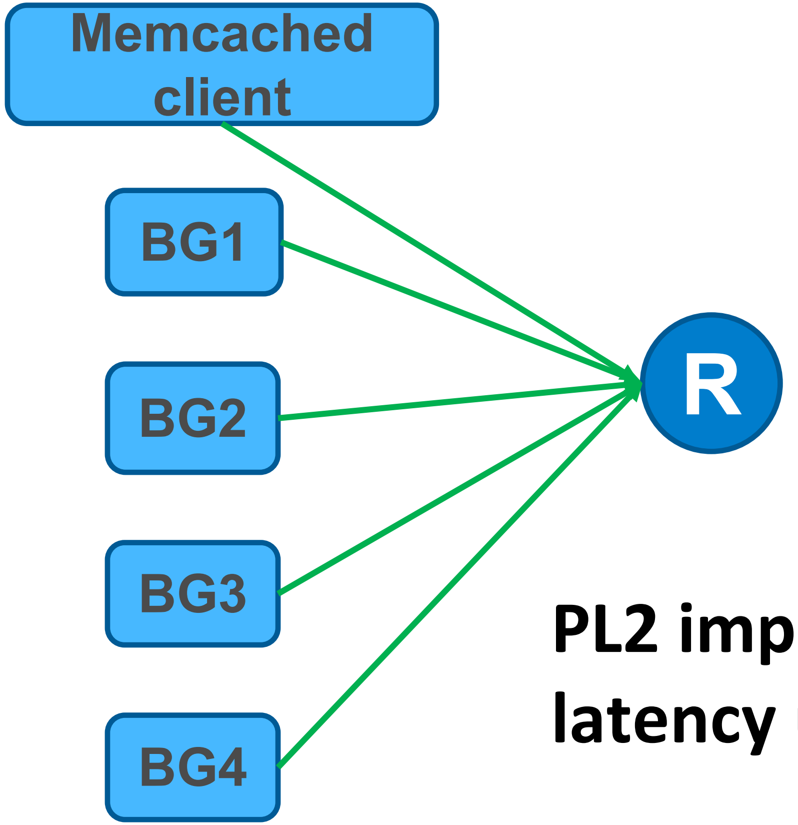
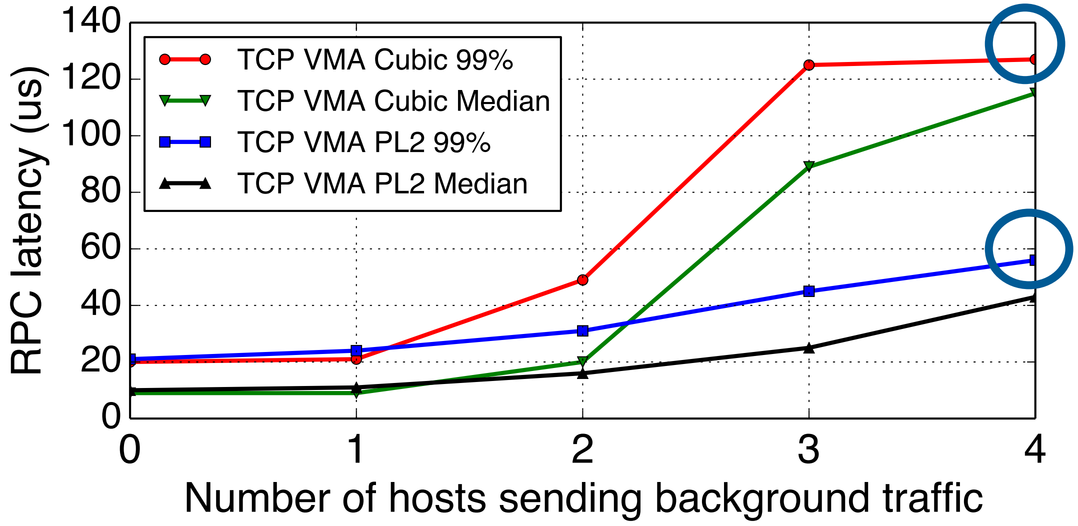
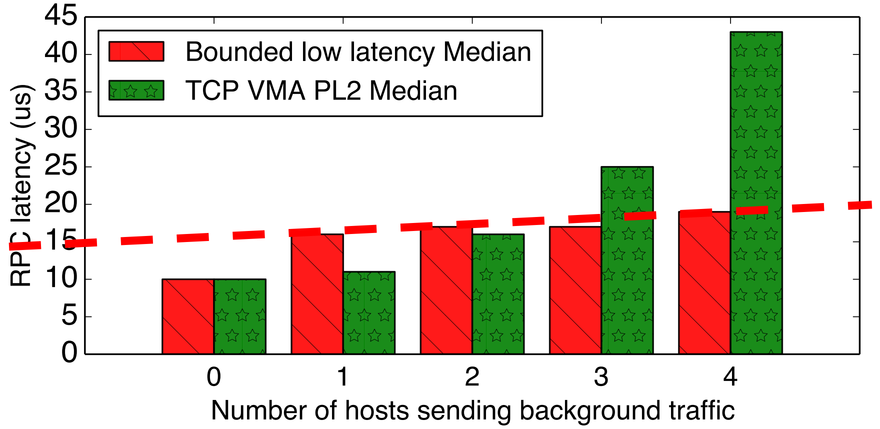
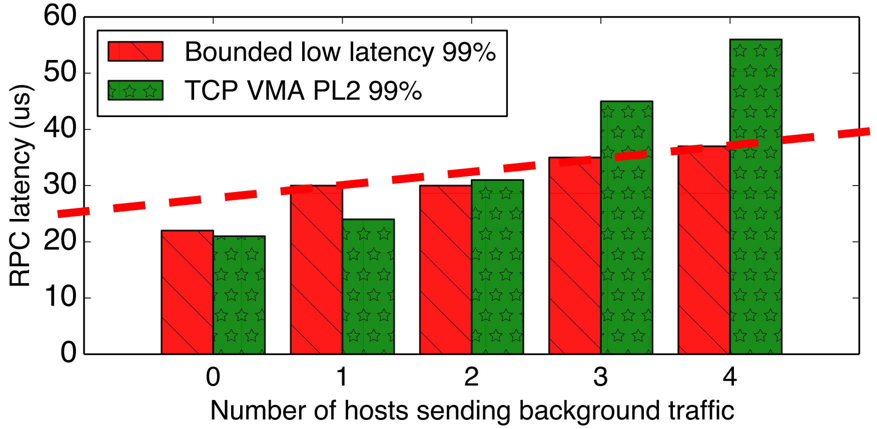




PL2 improves the 99th-percentile RPC latency up to 3X compared with Cubic.

Memcached (Bounded Low Latency)





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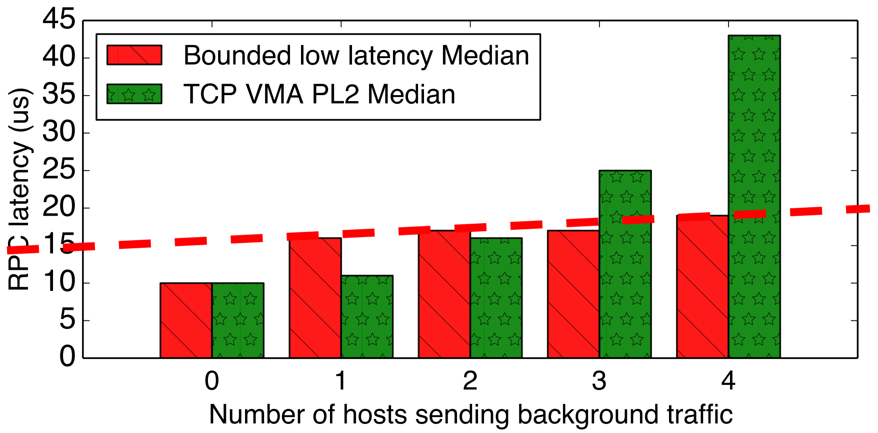

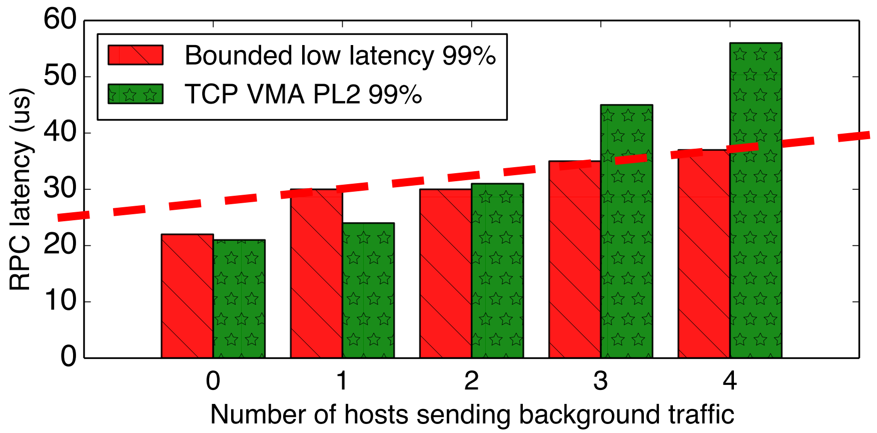

PL2 bounds message latency regardless of heavy background traffic.

Summary

- PL2 is a centralized packet scheduler towards the predictable low latency network in rack-scale network
- Co-design the switch logic and end host logic
    - Reduce the packet scheduling overhead
    - Bounded low latency for high priority message

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Thank You

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