

Speeding up Network FPGA Design using P4

Miroslaw Walukiewicz, Intel Bert Klaps, Intel

P4 can address multiple use-cases in mobile infrastructure



CU: Centralized Unit DU: Distributed Unit RU: Radio Unit AMF: Access and Mobility Management Function SMF: Session Management Function UDM: Unified Data Management UPF: User Plane Function CSR: Cell Site Router FEC: Forward Error Correction FHGW: Fronthaul Gateway HPS: Hard Processor System RAN: Radio Access Network PAC: Programmable Acceleration Card CPRI: Common Public Radio Interface

Example O-RAN connectivity enforcement

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P4 for vCSR – example of custom architecture

MPLS/SR-MPLS/SRv6 router core as pure P4 code





Source: Programming a target with P4 by p4.org

clock synchronization + QoS + FHGW as P4 extern objects

CSR: Cell Site Router FHGW: Fronthaul Gateway HPS: Hard Processor System QoS: Quality of Service RAN: Radio Access Network

P4 Integration with commercial router stack



Control + ex	ception	path
Forwarding	path	

Commercial router stack used as control plane Native Intel[®] FlexRAN stack integrated for vDU

Summary – FPGA is easy with P4

- Working vCSR example in FPGA completed in 6 months by engineers without RTL skills
 - Most of work spent on aligning P4 code for commercial MPLS pipeline
- Using well-defined host interfaces makes P4 based designs compatible with commercial applications like Intel[®] FlexRAN and commercial routing planes
- P4 tool can also be used for SRv6 and new use-cases such as network slicing
- Challenges:
 - P4 custom architecture in FPGA is not standardized
 - Externs are still in RTL
 - Work on simulation is ongoing BMv2 is very limited
 - Need to integrate with standard tools like Intel[®] P4 SDE



Thank You